

LCFC Confidential

BL460

(L460)


NM-A651 Rev1.0 Schematic

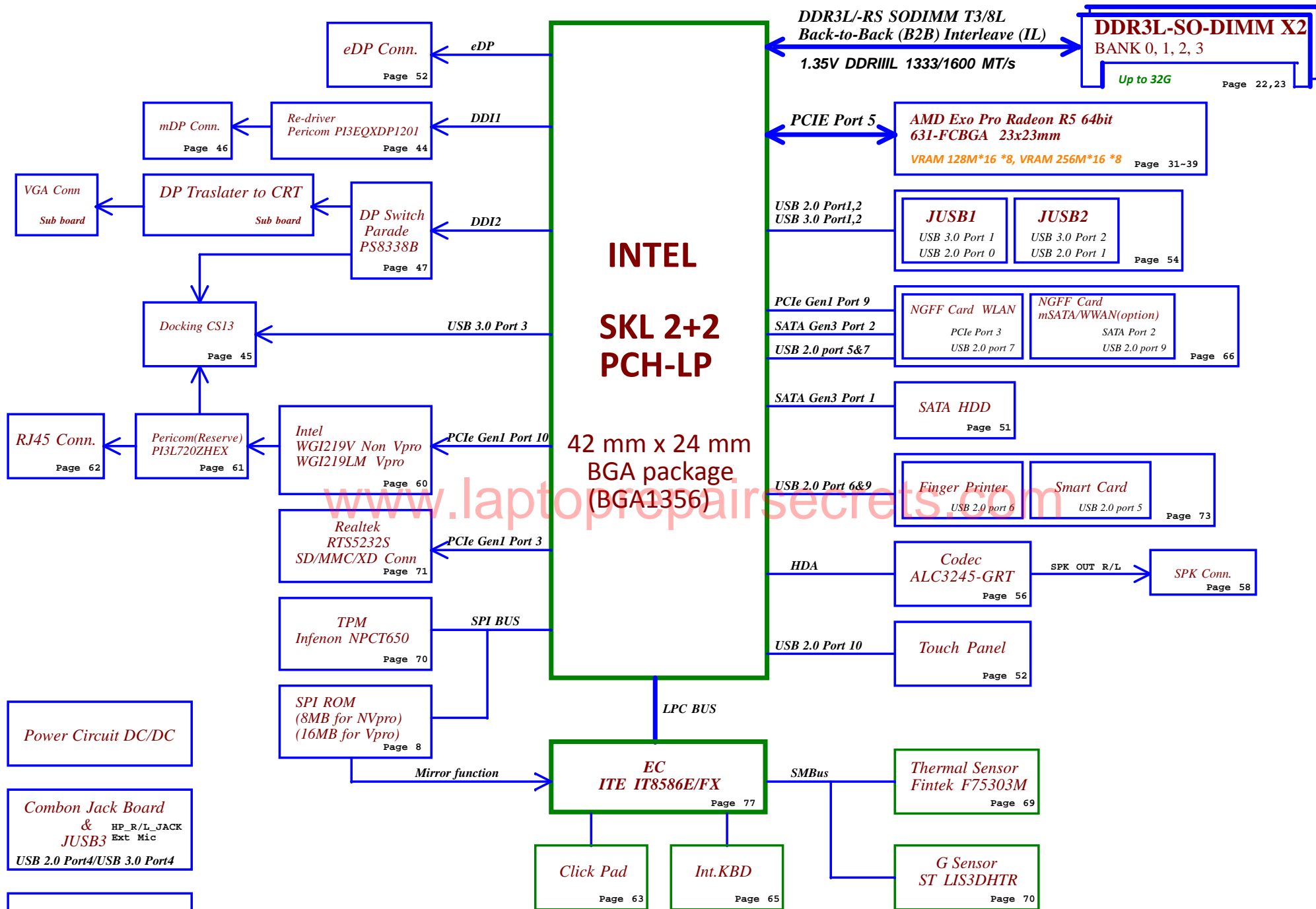
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Intel SKL Processor with DDRIII L + PCH

AMD Exo Pro Radeon R5 64bit

2015-10-22 Rev1.0

Security Classification	LC Future Center Secret Data			Title		
Issued Date	2015/01/12	Deciphered Date	2016/01/12	COVER PAGE		
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Voltage Rails

O --> Means ON
X --> Means OFF

Power Plane / State	B+	+1VALW +3VALW +1.8VALW +5VALW	+1.35V +0.675VS +VCC_ST	+5VS +3VS +VCC_CORE +VCC_GT +VCC_SA +VCC_IO +VCC_STG +VGA_CORE +1.5VS +0.95VS_VGA +1.5VS_VGA +1.8VS_VGA +3VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL						
	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	VM_PWRON	EC_ON	SUSP#
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S1 (Power on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	ON	OFF

SMBUS Control Table

	SOURCE	Main VGA	BATT	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	CP Module	Security ROM	LAN PHY
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL	X	V +3VALW	X	X	X	X	X	X	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3V_PCH	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3V_PCH	X	X	V +3VS	V +3VS	V +3VS	X	V +5VS	V +3VS	X
PCH_SML0_CLK PCH_SML0_DAT	PCH +3V_PCH	X	X	X	X	X	X	X	X	V +3VALW

HSIO Port

Port	Device
1	USB3.0 port (On Board)
2	USB3.0 port (On Board)
3	USB3.0 port (Docking)
4	USB3.0 port (Sub Board)
5	N/A
6	N/A
7	PCIE (Card Reader)
8	N/A
9	PCIE (GPU)
10	PCIE (GPU)
11	PCIE (GPU)
12	PCIE (GPU)
13	PCIE (WLAN)
14	PCIE (LAN)
15	SATA (HDD)
16	SATA (NGFF)

USB2.0 Port

Port	Device
1	USB port (On Board)
2	USB port (On bBoard)
3	USB port (Docking)
4	USB port (Sub Board)
5	WWAN
6	Finger Printer
7	BT
8	Camera
9	Smart Card
10	Touch Panel

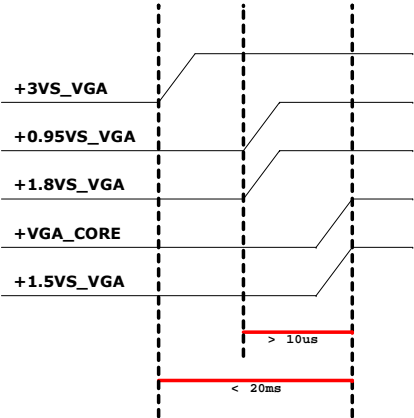
VGA GPIO (EXO-PRO-S3)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	N/A	
GPIO5	IN		GPIO5_AC_BATT
GPIO6	IN		GPIO6
GPIO7	OUT	N/A	
GPIO8	OUT	N/A	GPIO8_ROMSO
GPIO9	OUT	N/A	GPIO9_ROMSI
GPIO10	OUT	N/A	GPIO10_ROMSCK
GPIO11	OUT	N/A	
GPIO12	OUT	N/A	
GPIO13	OUT	N/A	
GPIO15	IN		SVI2_SVD
GPIO16	OUT	N/A	
GPIO17	OUT	N/A	
GPIO19	OUT	N/A	GPIO19_CTF
GPIO20	IN		SVI2_SVC
GPIO21	OUT	N/A	
GPIO22	OUT	N/A	GPIO22_ROMCSB
GPIO29	OUT	N/A	
GPIO30	OUT	N/A	

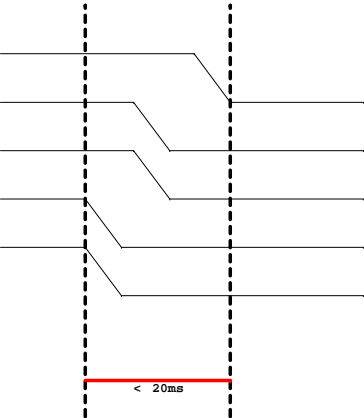
BOM Structure Table

BOM Structure	NOTE
PCB@	For PCB load BOM
3G@	3G function with WWAN
DIS@	Discreate SKU
UMA@	UMA SKU
DPRE@	With DP re-driver
NODPRE@	Bypass DP re-driver
NVPRO@	For Non-VPRO function
VPRO@	For VPRO function
MIRROR@	For mirror function
TPM@	TPM function
X76@	GPU VRAM Setting
XDP@	XDP function
EXO@	EXO function
ME@	ME Connector
EMC@	For EMC function
EMC_NS@	For EMC function (no mount)
RF@	For RF function
RF_NS@	For RF function (no mount)

GPU POWER UP sequence

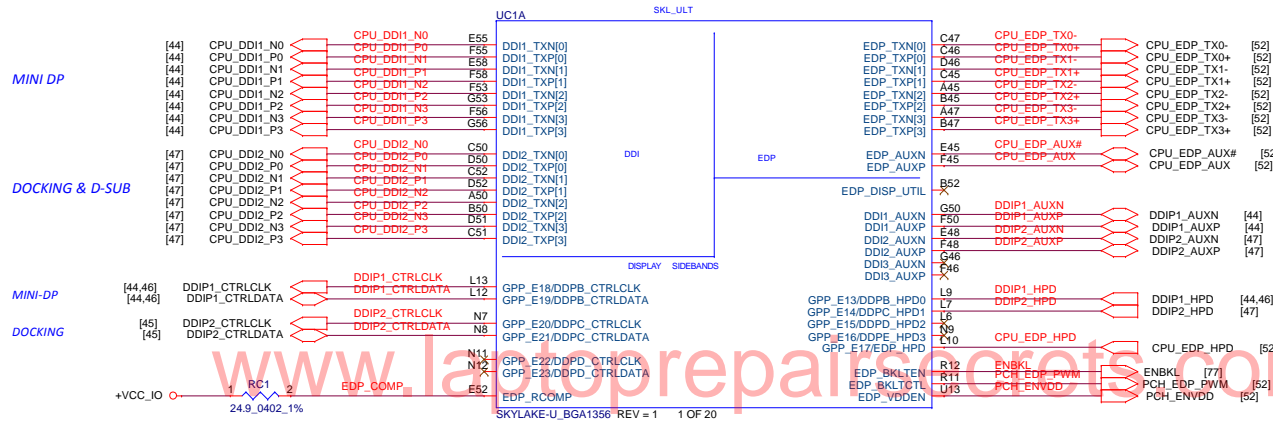


GPU POWER DOWN sequence

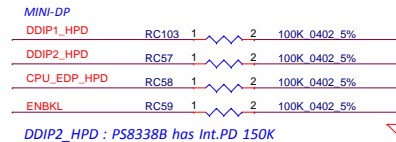
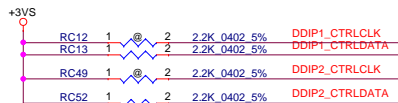


	Device ID
EXO-pro	6660

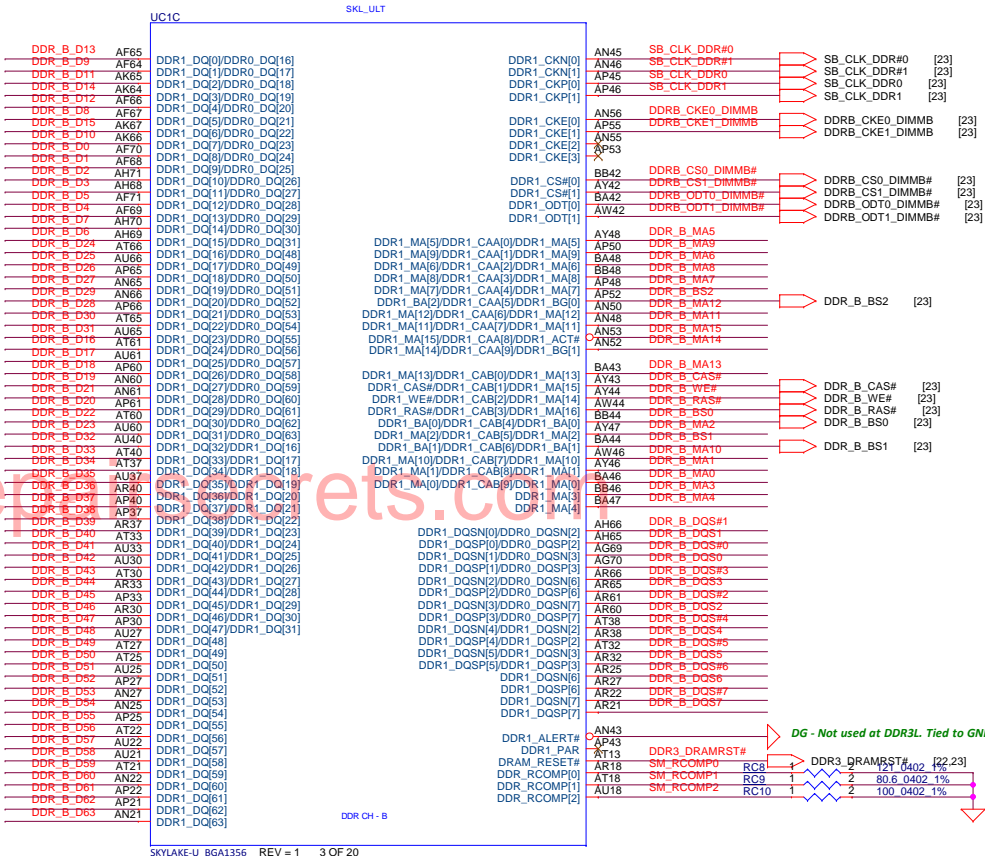
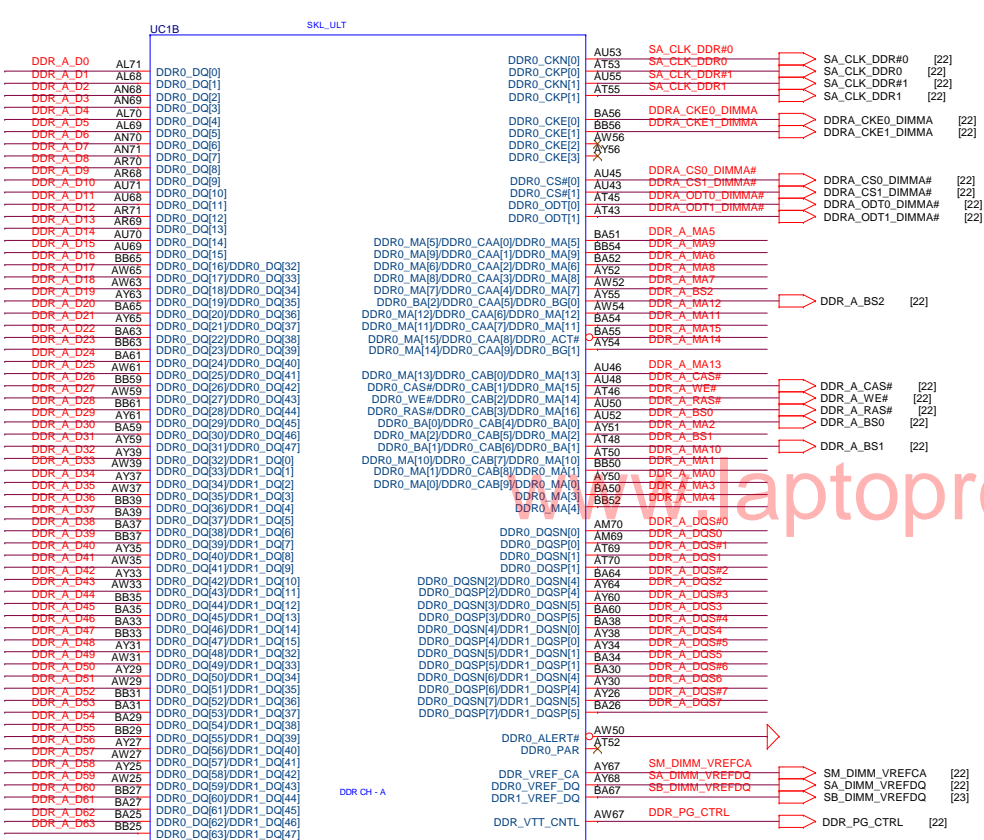
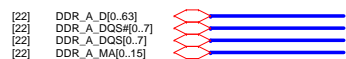
GPU		EXO-Pro-S3	
VRAM (GDDR3)		PS_3 (RV104)	PS_3 (RV105)
Samsung 1000MHz	K4W4G1646E-BC1A (2G)	PH 3.4K	PD 10K
	H5TC4G63CFR-N0C (2G)	PH 4.75K	NC
Hynix 1000MHz	MT41J256M16HA-093G:E (2G)	PH 3.24K	PD 5.62K




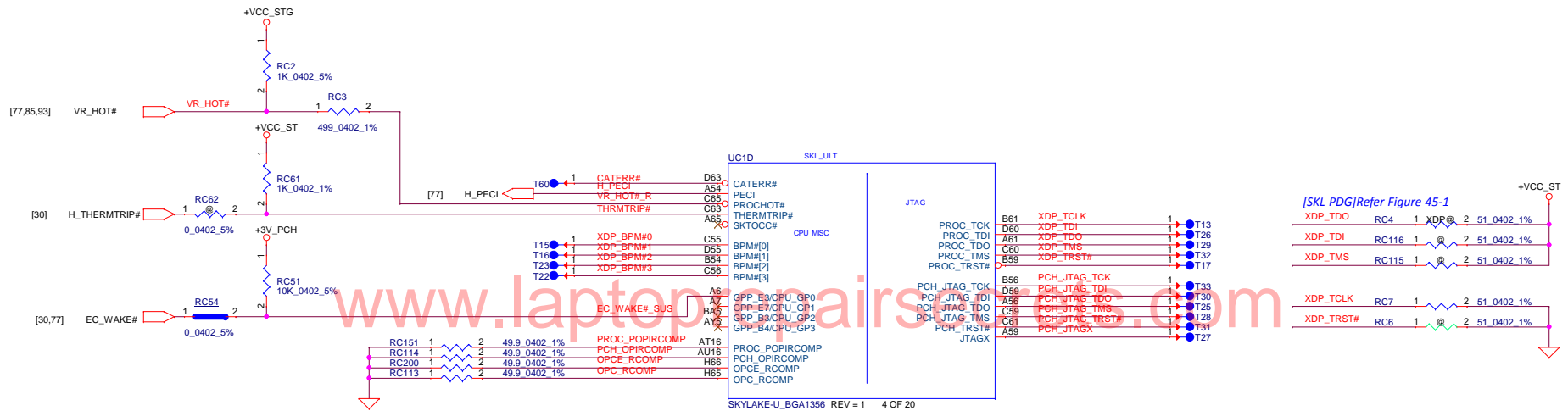
EDP_RCOMP
1. Trace width=20 mils, Spacing=25mil, Max length=100mils
2. RC1 close to MCP
Trace Width=20mil, Spacing=25mil, Max length=100mil



DP port	Enable	Disable
DDPB_CTRLDATA	pull-high	no connect
DDPC_CTRLDATA	pull-high	no connect



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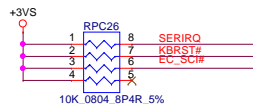
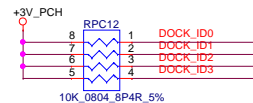


The diagram shows the pinout for the SD30000370T component in two packages: RP05 and RP07. The RP05 package is a 5-pin package, and the RP07 package is a 7-pin package. The pins are numbered 1 through 5 for RP05 and 1 through 7 for RP07. The connections are as follows:

Pin	RP05 Signal	RP07 Signal
1	SPI_I03_8MB	SPI_I03_4MB
2	SPI_CLK_8MB	SPI_CLK_4MB
3	SPI_SI_8MB	SPI_SI_4MB
4	SPI_I02_8MB	SPI_I02_4MB
5	SPI_I02_8MB	SPI_I02_4MB
6	SPI_SI_8MB	SPI_SI_4MB
7	SPI_CLK_8MB	SPI_CLK_4MB
8	SPI_I03_8MB	SPI_I03_4MB

Below the pinout diagrams, the component identifier and its specifications are listed:

33_0B04_8F4R_5%
SD30000370T



[70] SPI_CLK
 [70] SPI_SI
 [70] SPI_SO
 [70] SPI_CS2#_TPM

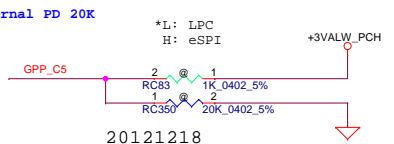
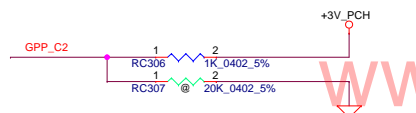
L:Disable Intel ME Crypto TLS cipher suite (no confidentiality).
 *H:Enable Intel ME Crypto Transport Layer Security (TLS) cipher
 suite (with confidentiality).Support Intel AMT with TLS and Intel
 SBA (Small Business Advantage) with TLS.

GPP_C2, Internal PD 20K

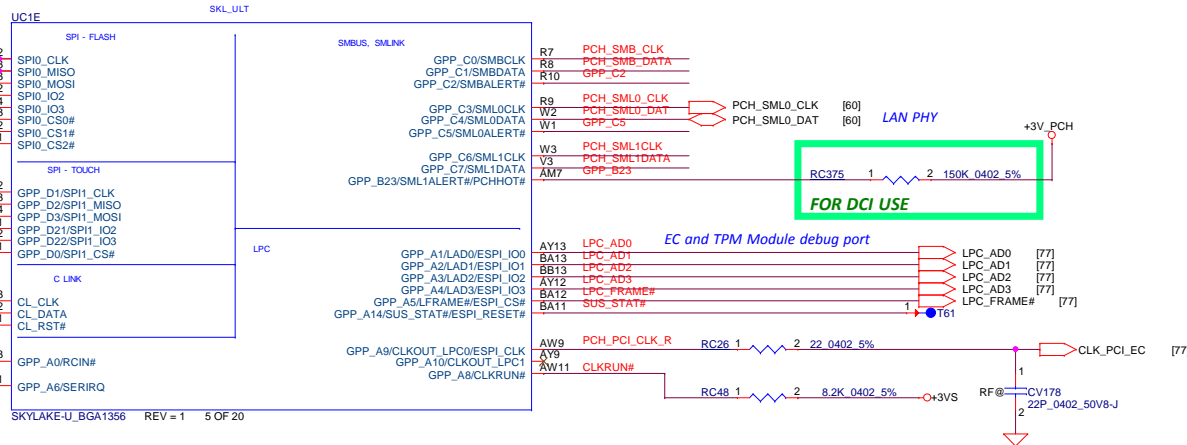
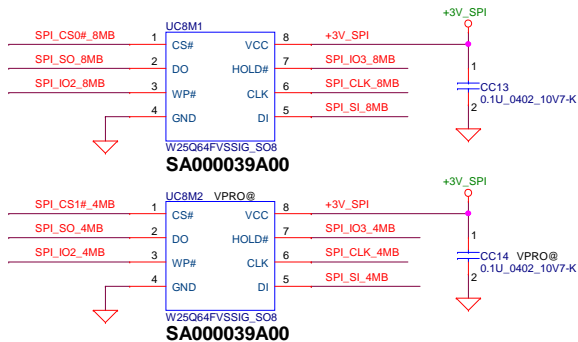
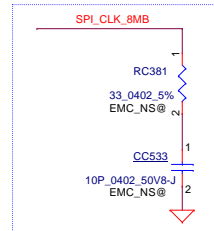
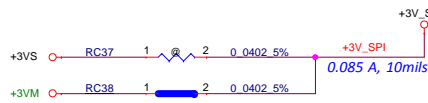
GPP_C5, Internal PD 20K

*L: LPC
 H: eSPI

20121218



- +3VM = +3V_SPI
- 1. VPRO : Q6, +3VLAW To +3VM
- 2. NVPRO :
 - a. R17 and RC38, +3VALW to +3VM

[illegible]

SMBus

*DIMM1, DIMM2
CP, Security ROM*

+3VS

RC35 1 2 4.7K .0402 5%

RC36 1 2 4.7K .0402 5%

PCH_SMB_CLK

PM_SMB_CLK

[22,23,63]

PCH_SMB_DATA

PM_SMB_DATA

[22,23,63]

QC1A
2N7002KDWH_SOT363-6
SB0000013A00

QC1B
2N7002KDWH_SOT363-6
SB0000013A00

**GPU, Thermal Sensor,
Embedded Controller, G sensor**

+3VS

PCH_SML1CLK

EC_SMB_CK3

[30,69,77,77]

PCH_SML1DATA

EC_SMB_DA3


[30,69,77,77]

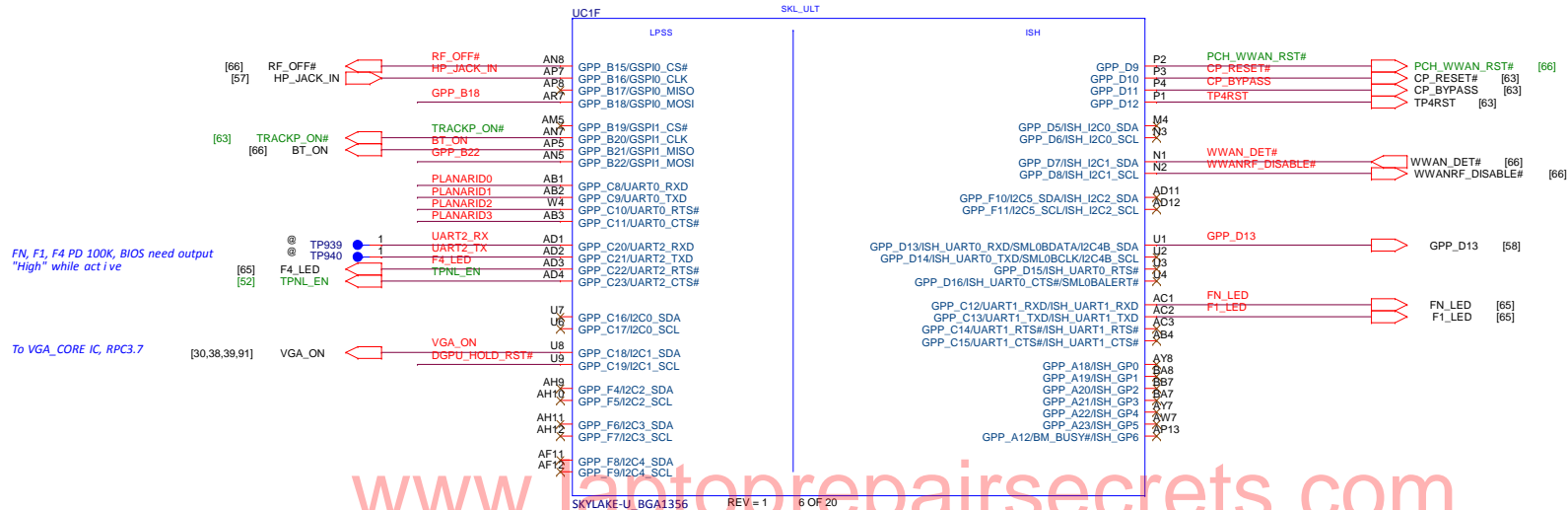
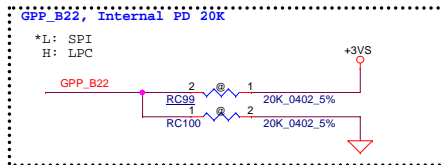
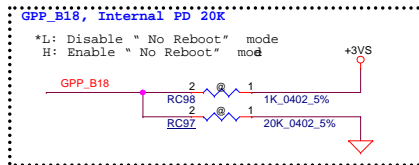
QC2A
2N7002KDWH_SOT363-6
SB0000013A00

QC2B
2N7002KDWH_SOT363-6
SB0000013A00

*2N7002KDWH
Vth= min 1V, max 2.5V
ESD 2KV*

Signal	Pin	Function	Level	Width	Period	Duty	Frequency
[77] FSCE#	RE1	FSCE#	1	2	0.0402	5%	SPI_CS0#_8MB
[77] SPI_FMO5#	RE2	SPI_FMO5#	1	2	0.0402	5%	SPI_ST_8MB
[77] SPI_FMO5	RE3	SPI_FMO5	1	2	0.0402	5%	SPI_SO_8MB
[77] SPI_FMSO	RE4	SPI_FMSO	1	2	0.0402	5%	SPI_CLK_8MB
[77] SPI_FSCK	RE4	SPI_FSCK	1	2	0.0402	5%	SPI_CLK_8MB

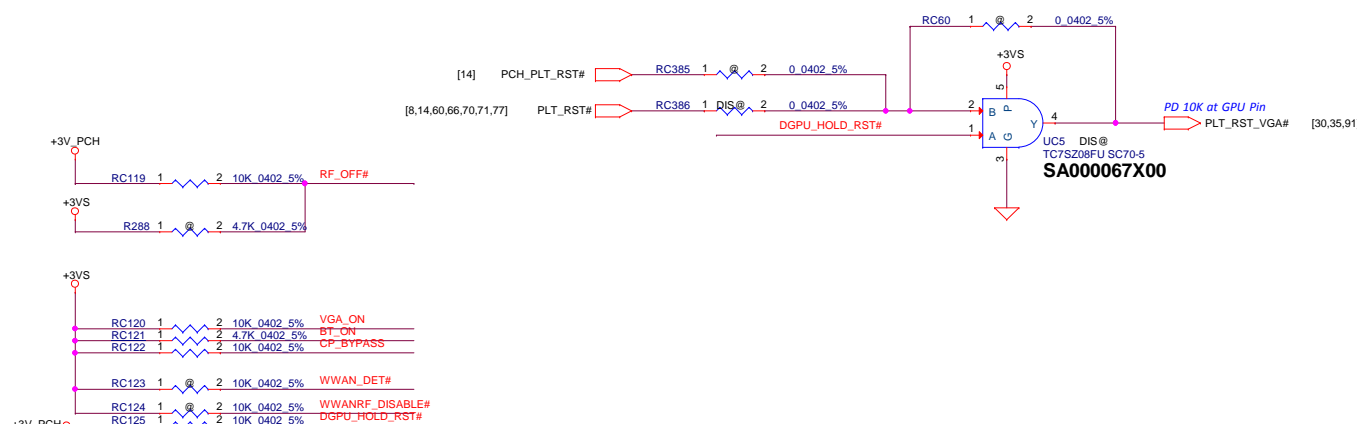
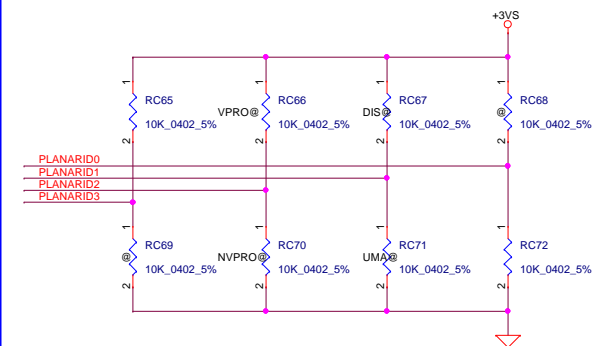
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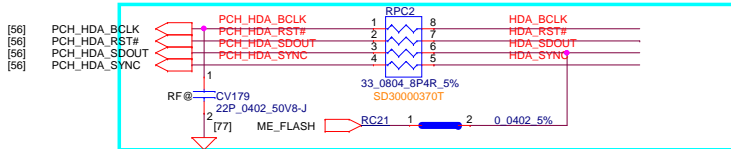
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Project/SKU ID

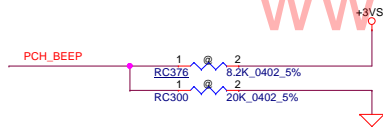
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1	1(RC65)	VPRO SKU (RC66)	DIS (RC67)	15" (RC68)
0	X	NVPRO SKU (RC70)	UMA (RC71)	14" (RC72)



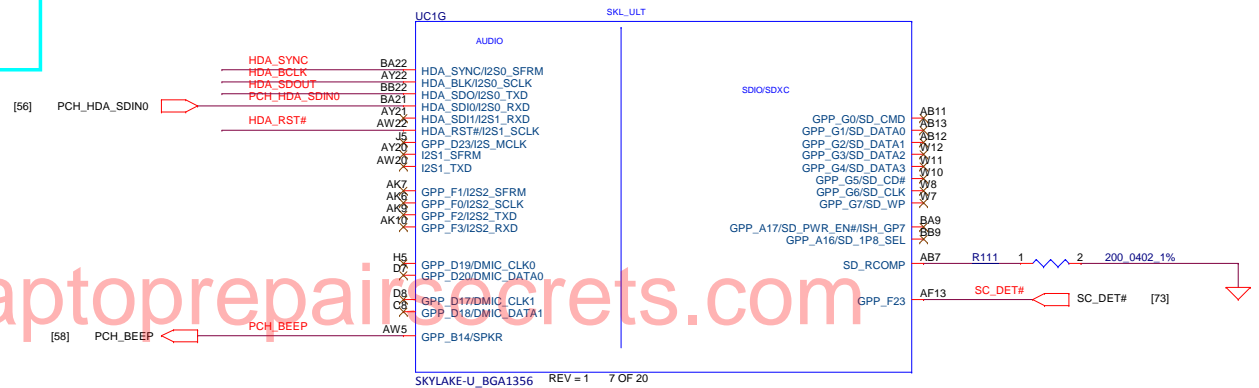
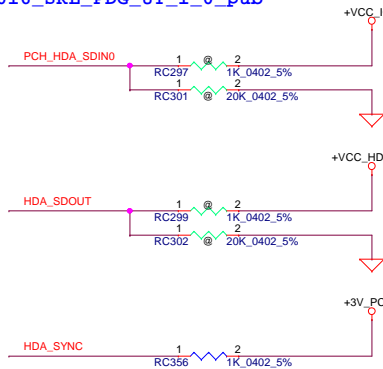
Need to check again?



GPP_B14, Internal PD 20K
No Reboot on TCO
Timer expiration
pull-up to VCC3_3 through a 1~8.2KΩ
resistor to disable this capability



Processor Strapping
543016_543016_SKL_PDG_UY_1_0_pub
P780



Card Reader

WLAN

LAN

HDD

SSD(NGFF)

GPU

UCH

SKL_ULT

PCIe/USB3/SATA

SSIC / USB3

USB2

SKYLAKE-U_BGA1356 REV = 1 8 OF 20

On Board (Right-Front)

On Board (Right-Back)

DOCKING

S/B (AOU Port)

On Board (Right-Front)

On Board (Right-Back)

DOCKING

S/B (AOU Port)

SMART CARD

Finger Printer

BT

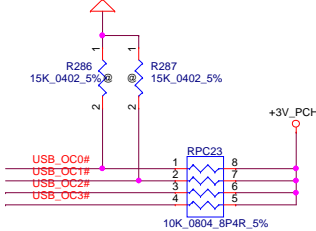
CAMERA

WWAN

Touch Panel

On Board (Right-Front)
S/B (AOU Port)

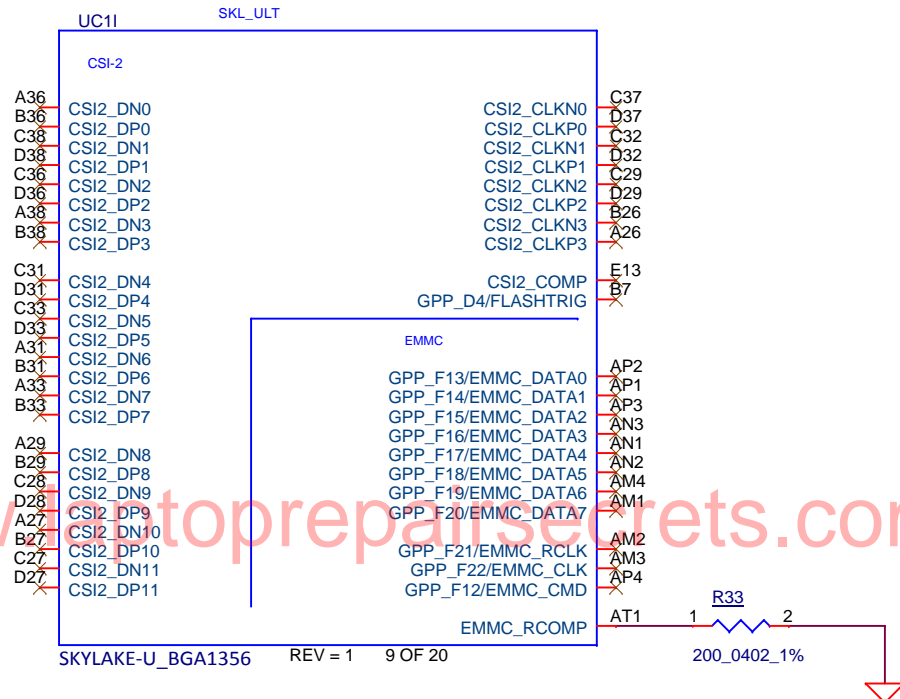
HDD_DEVSLOP0 RC377 2 @ 1 10K 0402 5%
SSD_DEVSLOP1 RC378 2 @ 1 10K 0402 5%




Pin.	USB3.0 Port NO.	USB2.0 Port NO.	Default Port Mapping
USB_OC0#	Port 1, 2	Port 0, 1	Port 0, 1
USB_OC1#	Port 4	Port 3	Port 2, 3
USB_OC2#	Unused.	Unused.	Port 4, 5
USB_OC3#	Unused.	Unused.	Port 6, 7

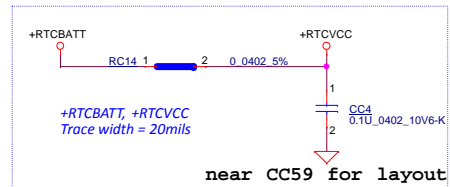
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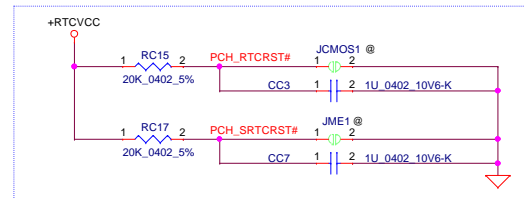


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Issued Date	2015/01/12	Deciphered Date	2016/01/12						
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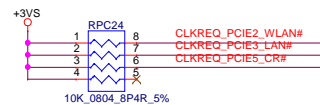
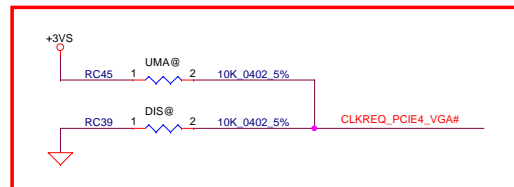
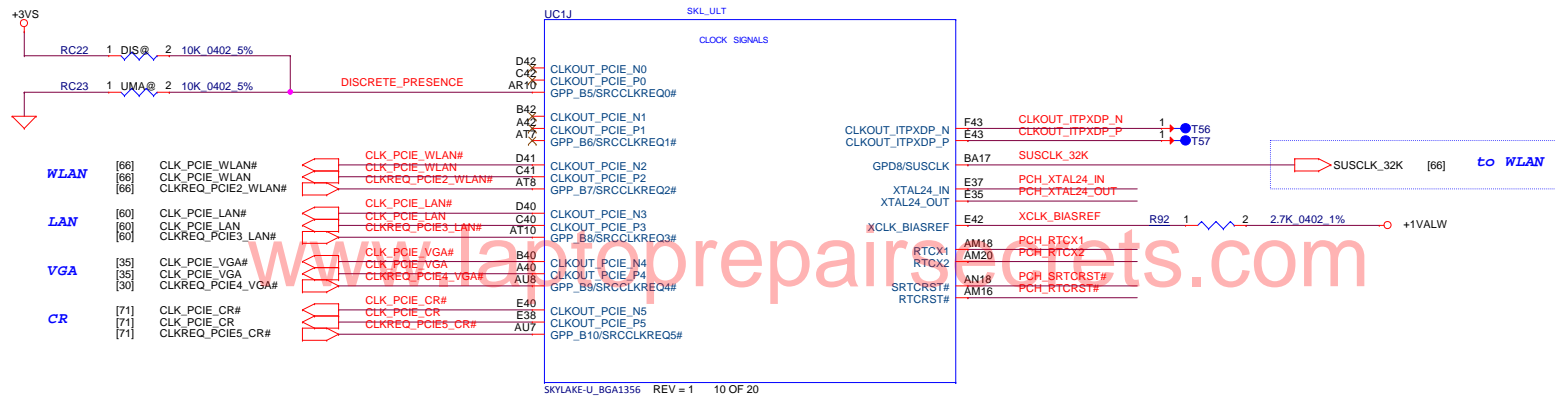
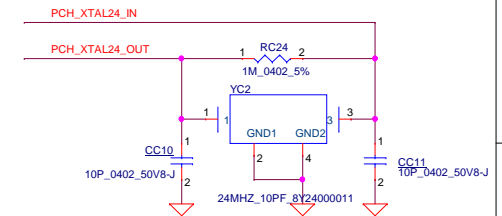
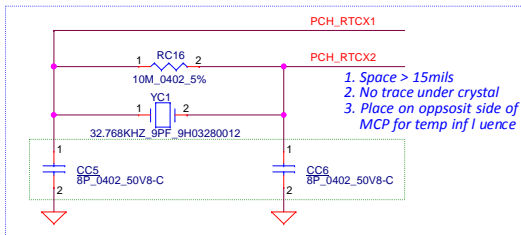
RTC External Circuit

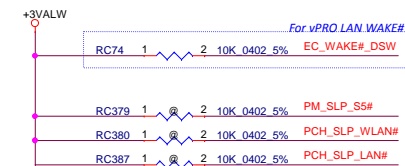
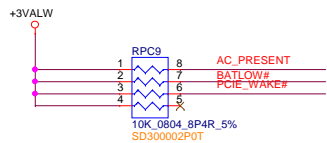
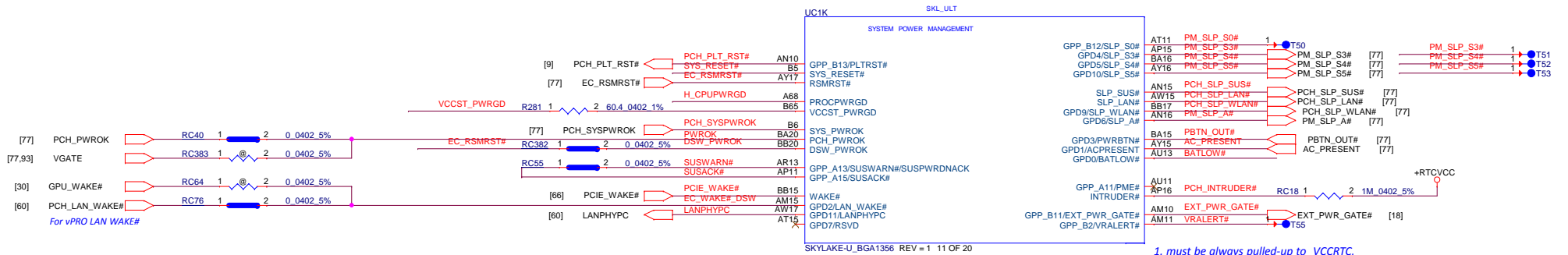


JCMOS, JME Set ting Need Under DDR Dao

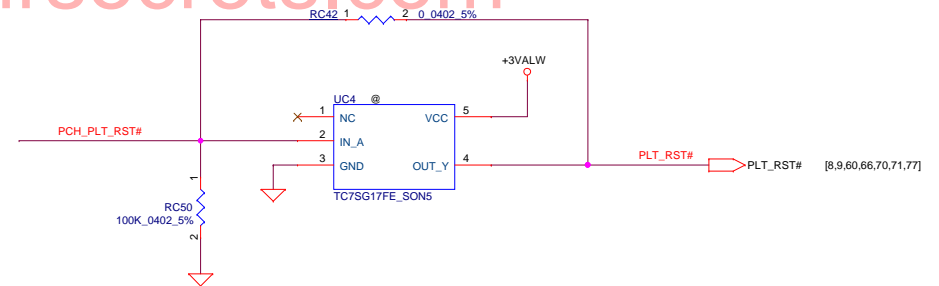
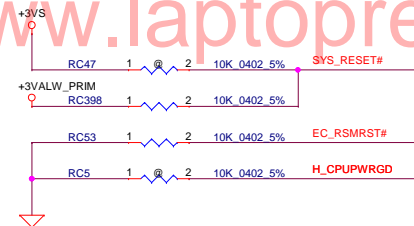


RTC Crystal

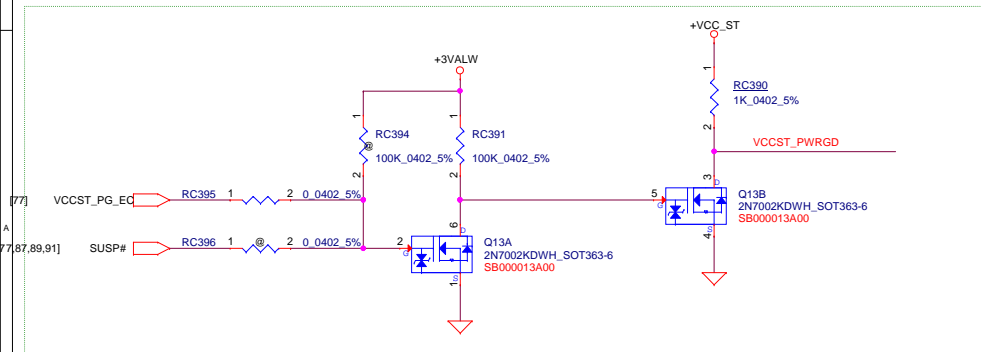




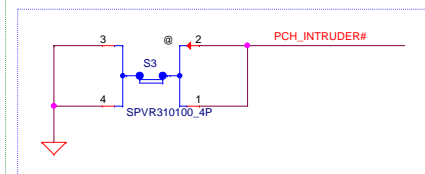
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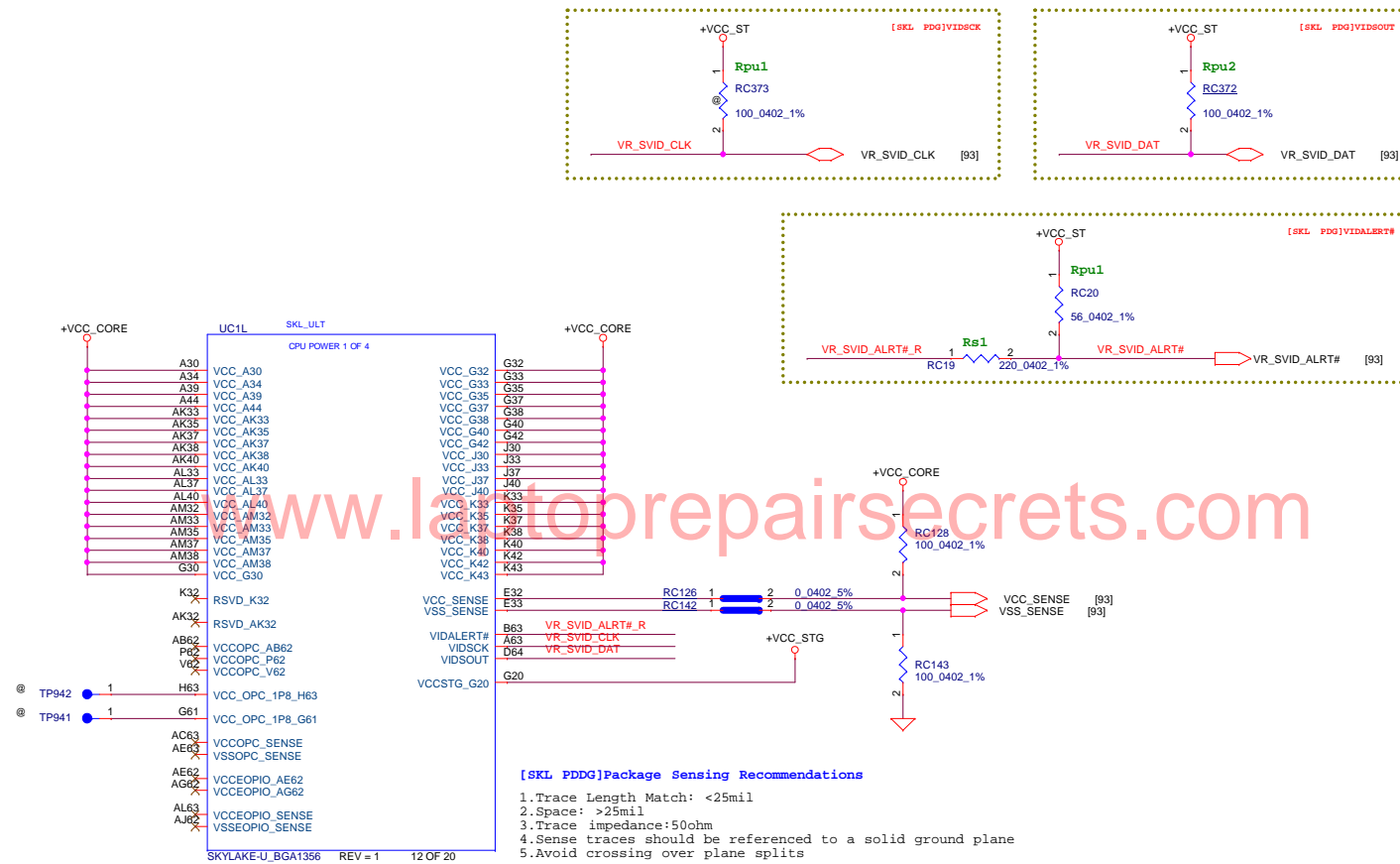
Reserved for HW control



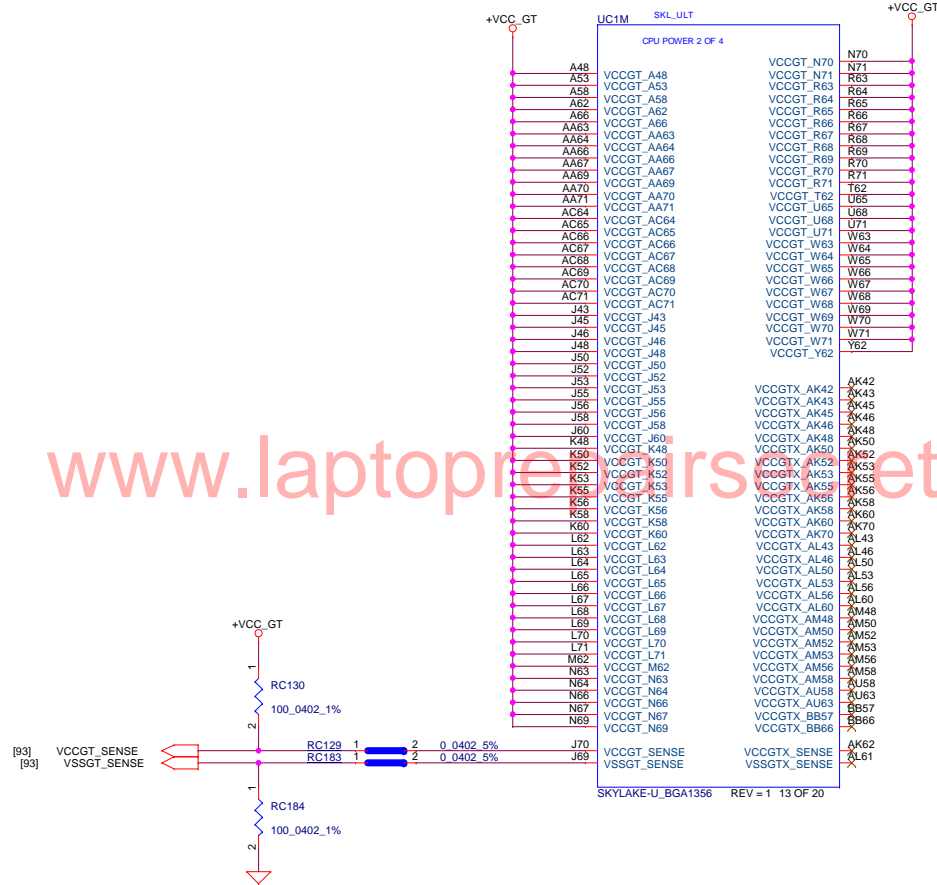
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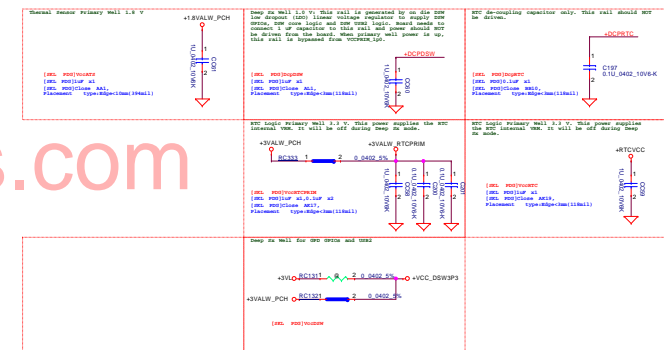
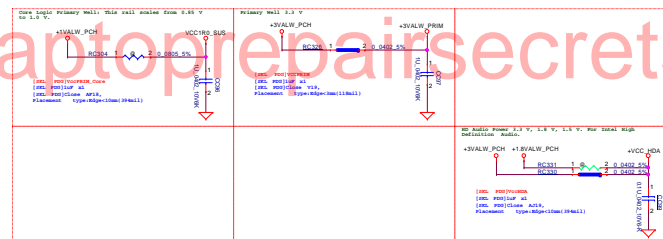
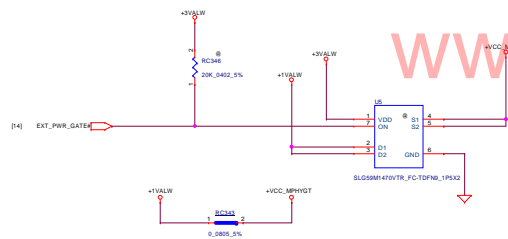
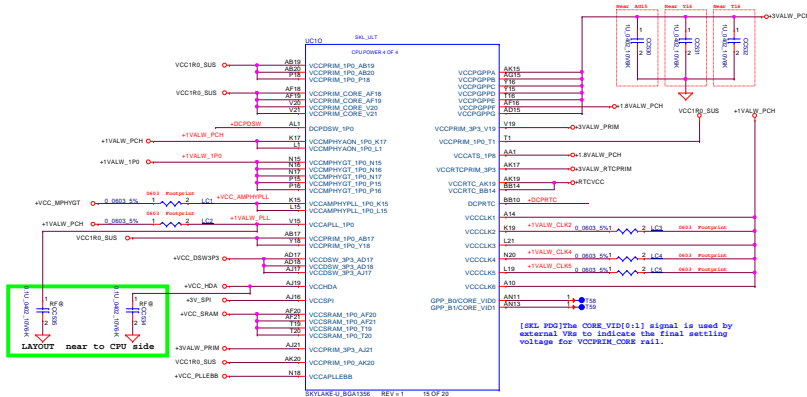
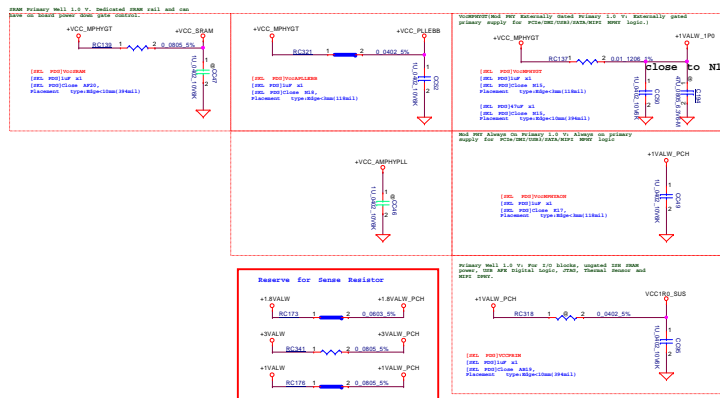


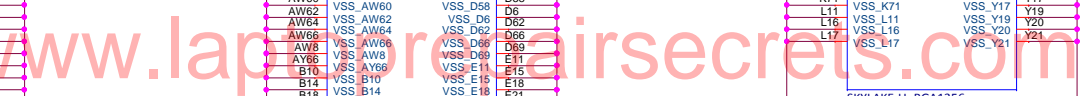
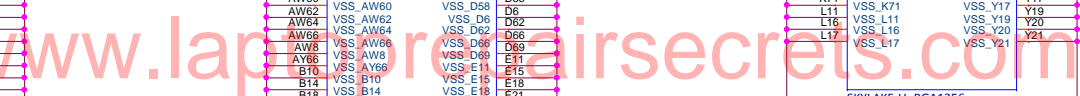
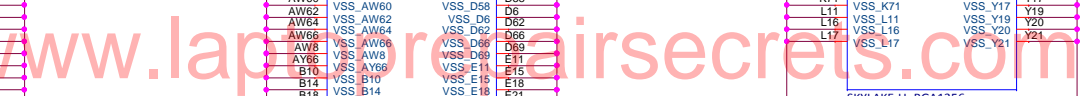
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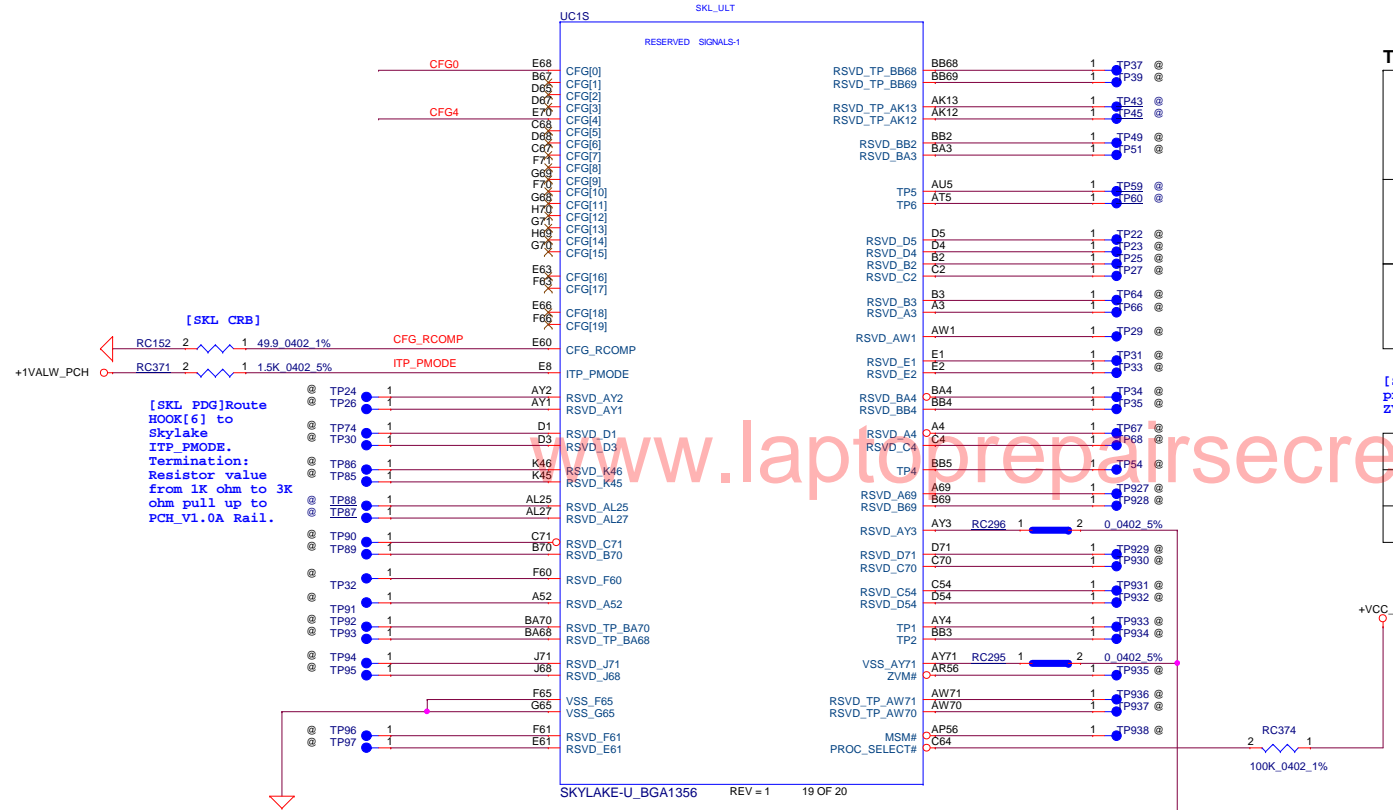


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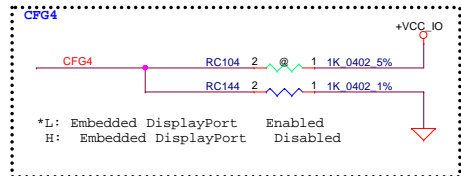
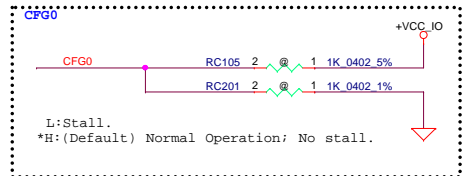








[SKL_EDS]



TABLE

CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted
1: No Stall
0: Stall

CFG4 : eDP Enable
1: Disabled
0: Enabled

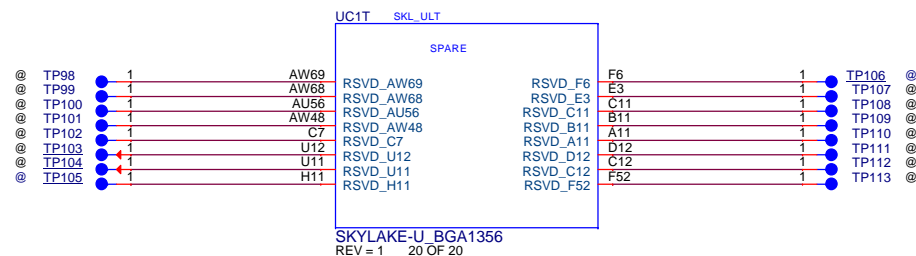
CFG9 : SVID Bus Communication
1: Enabled
0: Disabled

[SKL_EDS]Zero Voltage Mode:VCCOCP is fixed OPC VR output voltage of 1V, the processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal as shown below:


ZVM#	state	VCCOCP
0V		0V
1V		1V

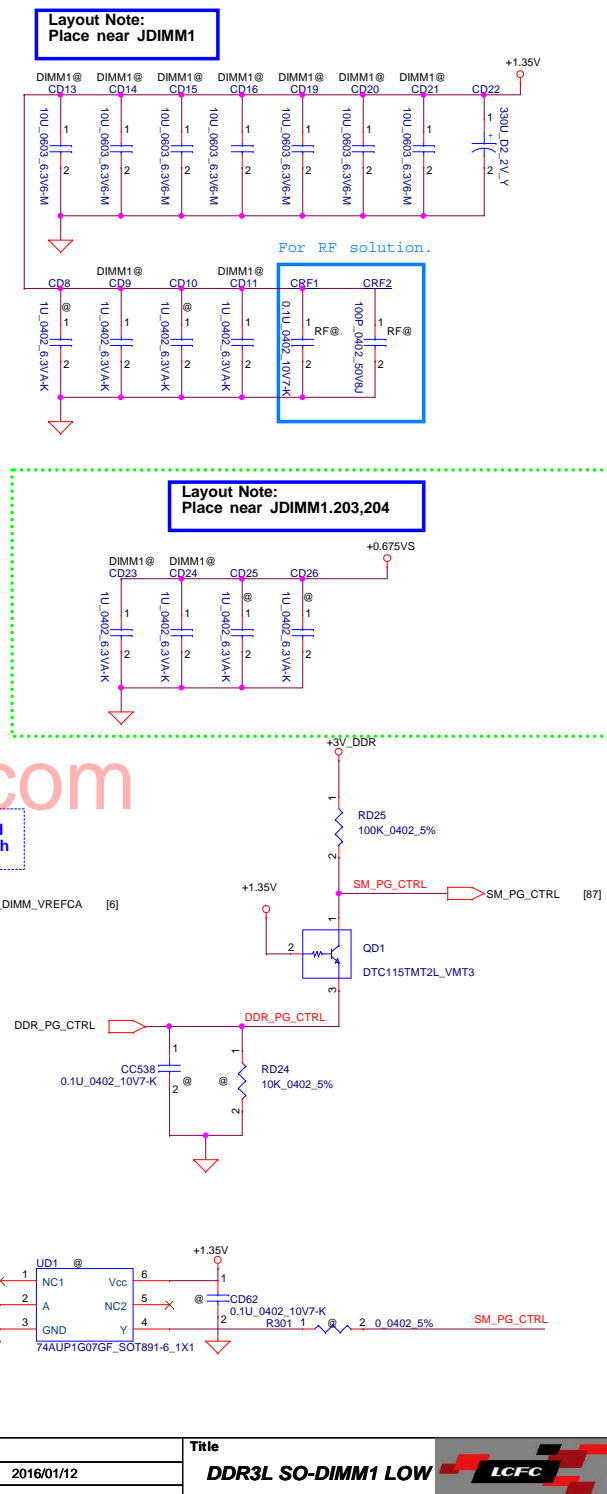
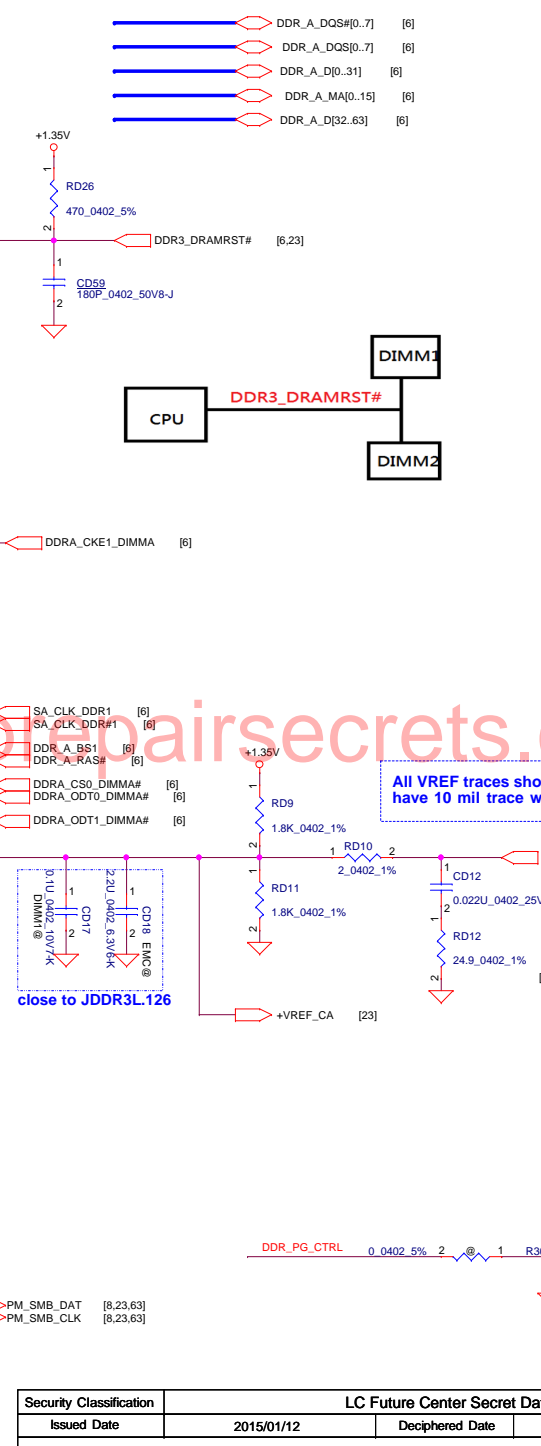
[SKL_EDS]Minimum Speed Mode: VCCEPIO can be connected to OPC VR in this case VCCEPIO is fixed to 1V. The processor can drive VR to LPM (Low Power Mode) which sets VR output to 0V using ZVM# signal. In order to achieve better power/performance it is recommended to use a separate VR for VCCEPIO in this case VCCEPIO is configurable to 0.8V/1V. The processor drives the VR to set VCCEPIO value(0.8V/1V) using MSM# signal, based on the required bandwidth for the BOPIO interface as shown below:

ZVM#	state	MSM#	state	VCCEPIO
0V		X		0V
1V		0V		0.8V
1V		1V		1V



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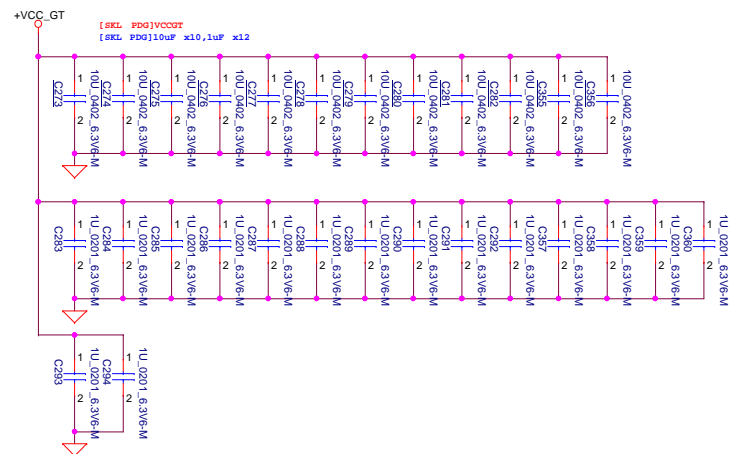


Channel A


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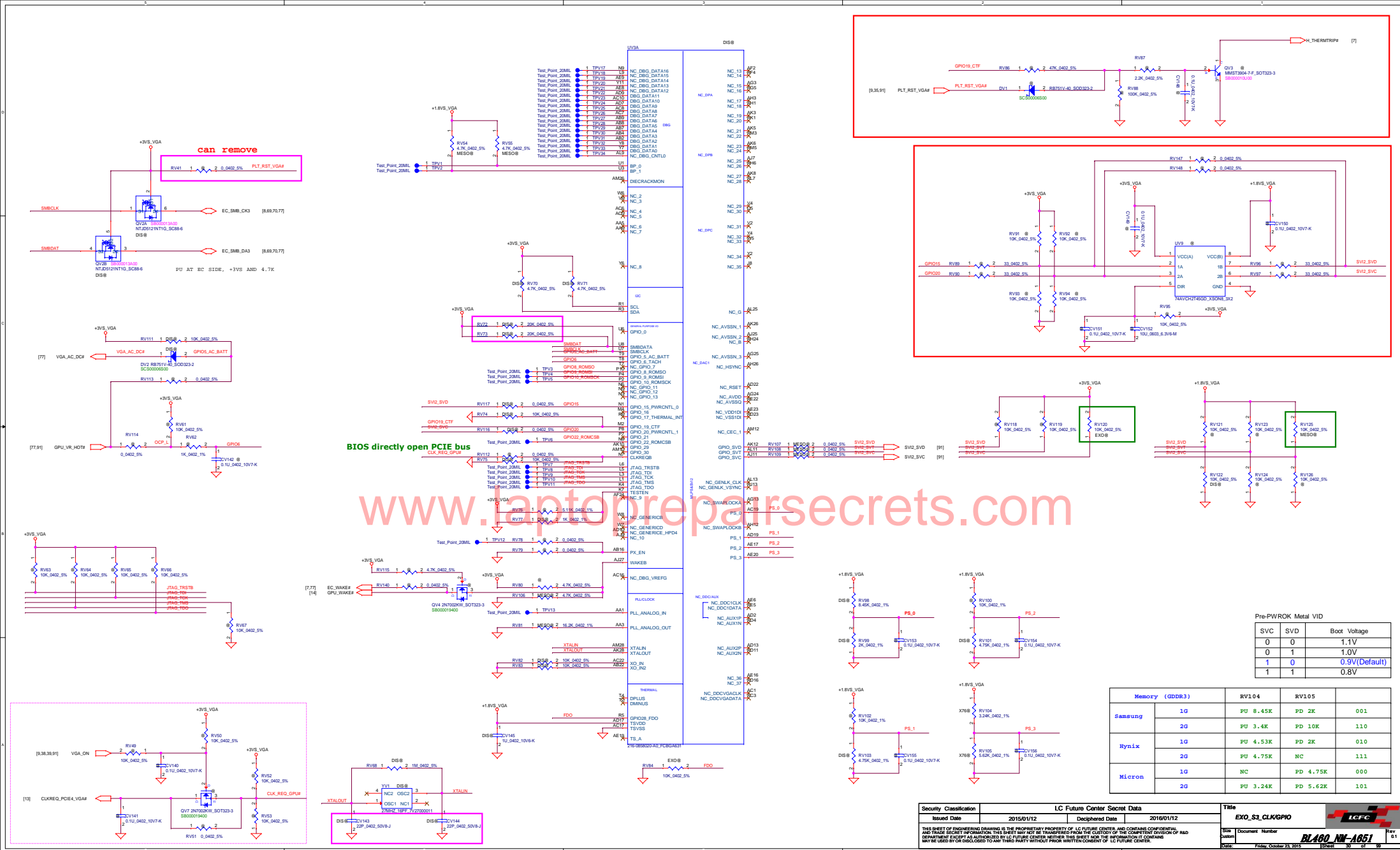
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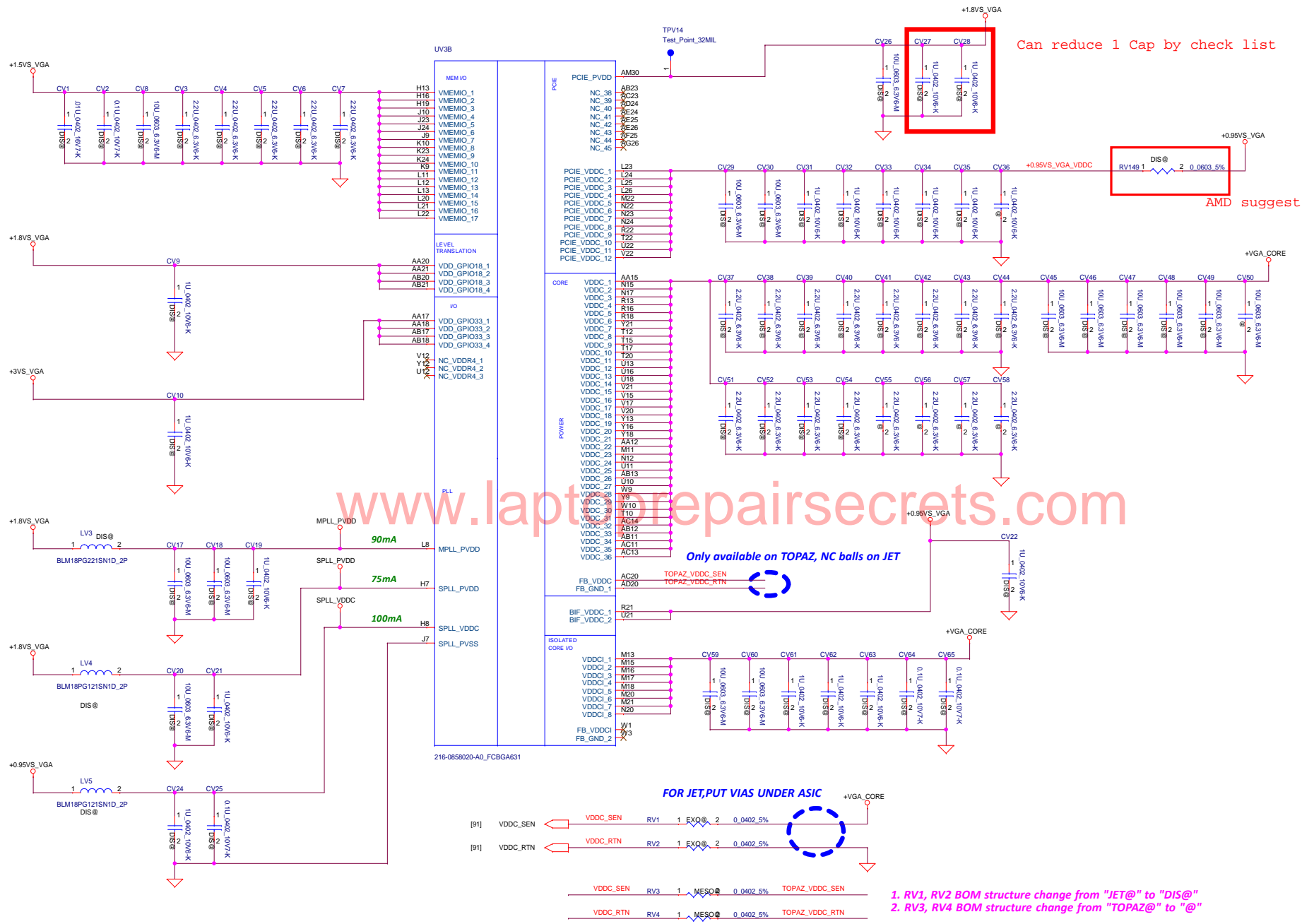
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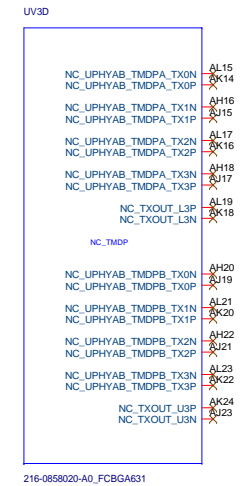
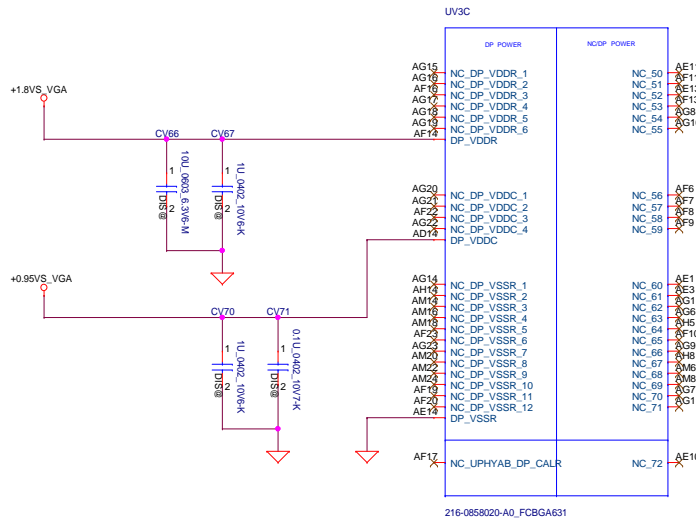
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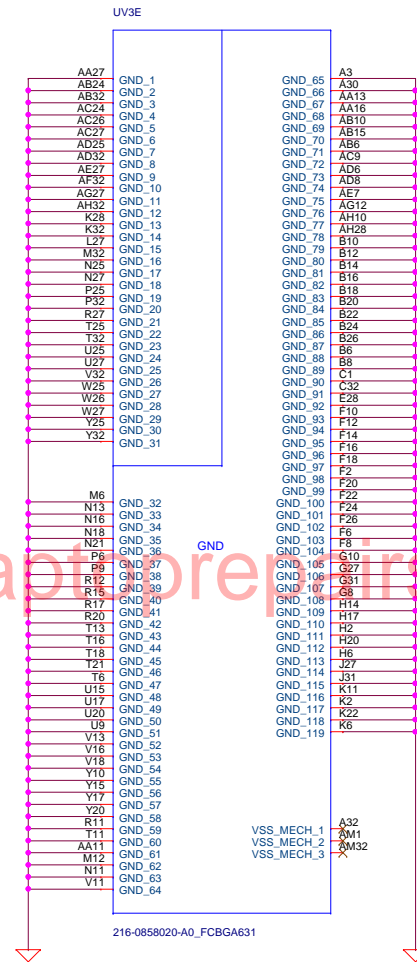


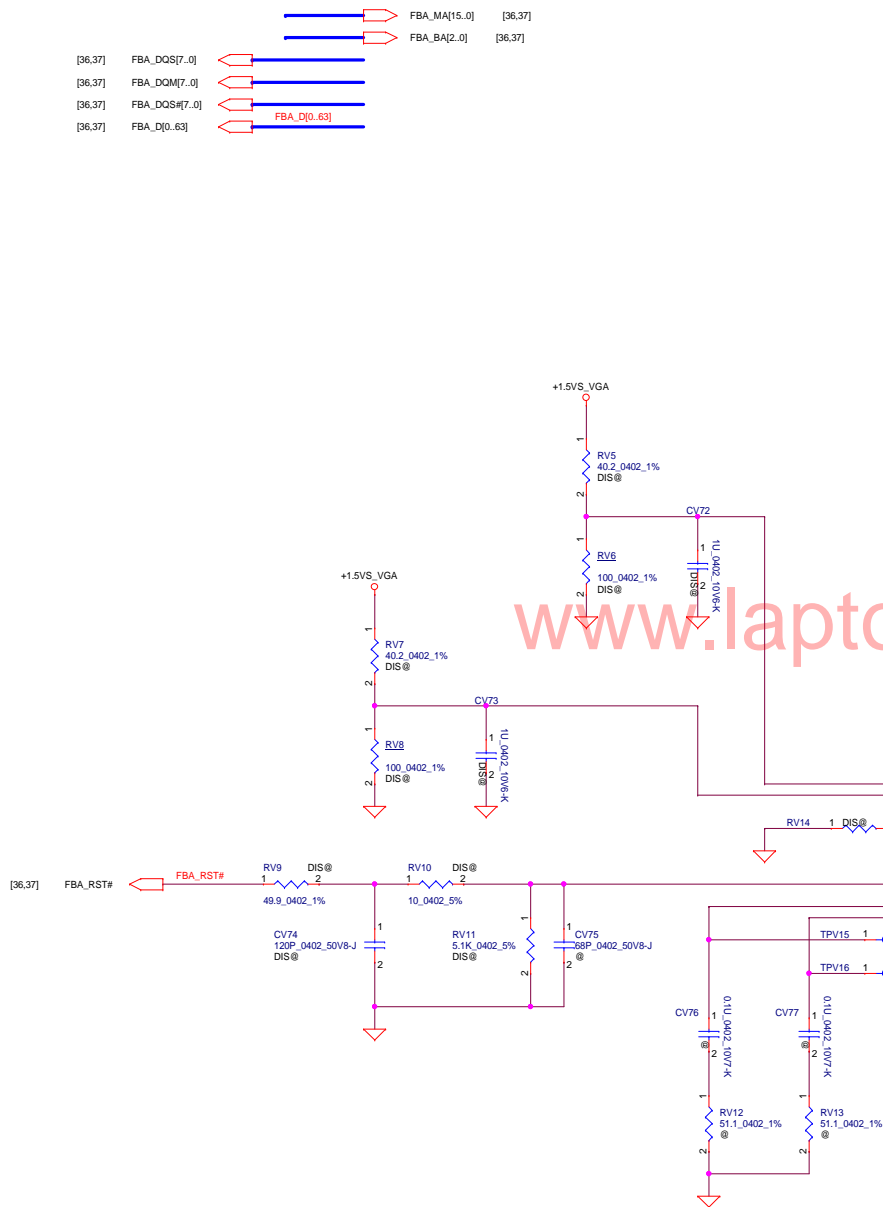
ASIC Ball	Topaz	Jet
U10, T10 AB13, W9 AB11, AB12 AC11, AC13 AC14, Y9, W10	VDDC	NC
AC20	FB_VDDC	NC
AD20	FB_VSS	NC
W1	FB_VDDCI	NC
W3	FB_VSS	NC
AJ11	GPIO_SVC	NC_SVI2
AK12	GPIO_SVD	NC_SVI2
AL11	GPIO_SVT	NC_SVI2
N6	GPIO_11	NC_GPIO11
N5	GPIO_12	NC_GPIO12
N3	GPIO_13	NC_GPIO13
AJ27	WAKEB	NC_VSYNC
T8	PCC/GPIO_6	GPIO_6
AA3	PLL_ANALOG_OUT	NC
AA1	PLL_ANALOG_IN	NC

ASIC Ball	Topaz	Jet
U1	BP_0	NC
U3	BP_1	NC
AM26	DIECRACKMON	NC
Y11	NC	DBG_DATA13
AE9	NC	DBG_DATA14
L9	NC	DBG_DATA15
N9	NC	DBG_DATA16
AE8	NC	DBG_DATA12
AL9	NC	DBG_CNTL0
H13, H16, H19, J10 J23, J24, J9, K10 K23, K24, K9, L11 L12, L13, L20, L21 L22	VMEMIO	VDDR1
AA17, AA18 AB17, AB18	VDD_GPIO33	VDDR3
AA20, AA21 AB20, AB21	VDD_GPIO18	VDD_CT

	Bits5	Bits4	Bits3	Bits2	Bits1
PS0	1	1	0	0	1
PS1	1	1	0	0	0
PS2	0	0	0	0	0
PS3	1	1	?	?	?

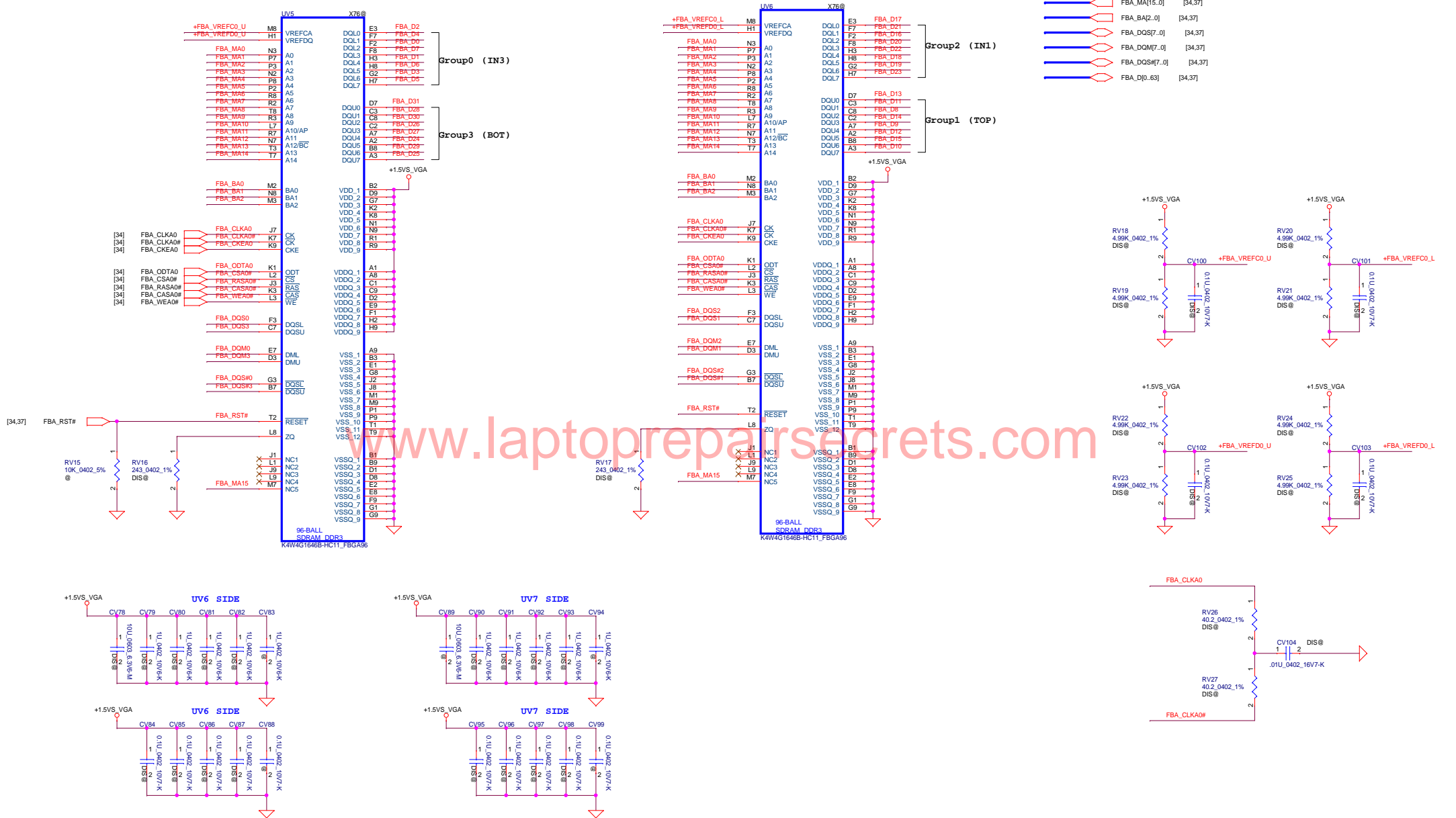
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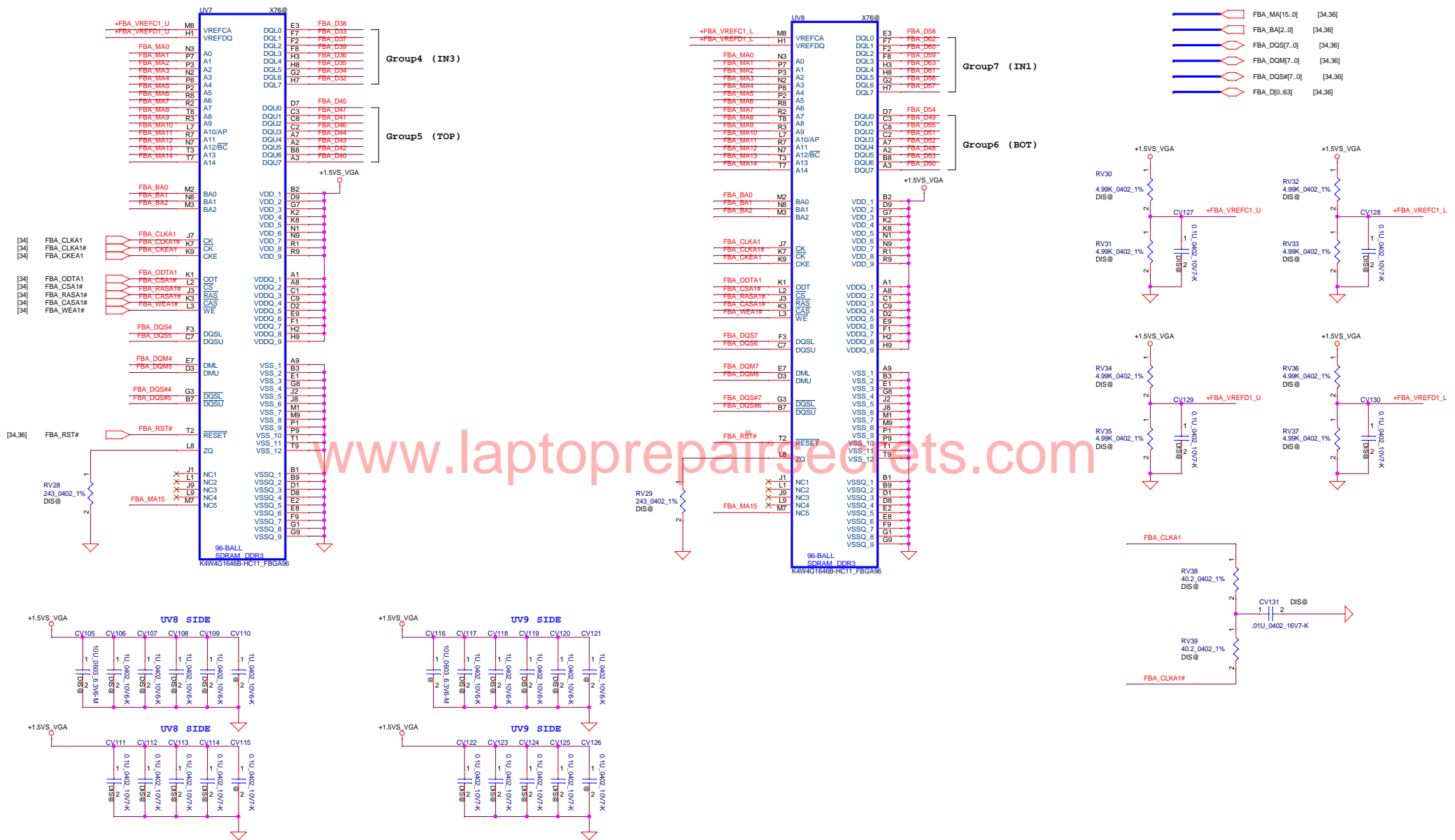



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FBA D6	F28	FBA D21	[36,37]
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FBA D266	A0		
FBA D267	C0		
FBA D268	E0		
FBA D269	D0		
FBA D270	F0		
FBA D271	A0		
FBA D272	C0		
FBA D273	E0		
FBA D274	D0		
FBA D275	F0		
FBA D276	A0		
FBA D277	C0		
FBA D278	E0		
FBA D279	D0		
FBA D280	F0		
FBA D281	A0		
FBA D282	C0		
FBA D283	E0		
FBA D284	D0		
FBA D285	F0		
FBA D286	A0		
FBA D287	C0		
FBA D288	E0		
FBA D289	D0		
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FBA D291	A0		
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FBA D408	E0		
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FBA D410	F0		
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FBA D413			

Memory Partition A - Lower 32 bits

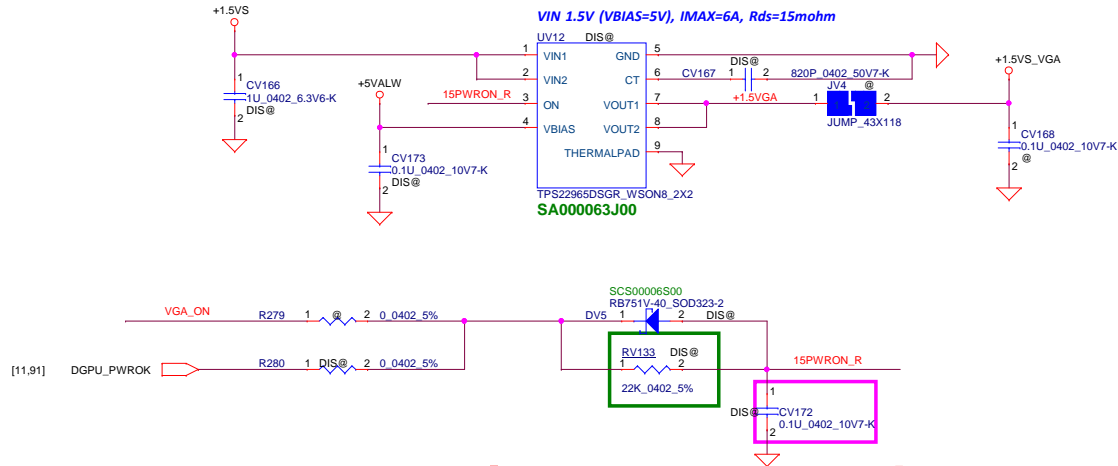


Memory Partition A - Upper 32 bits



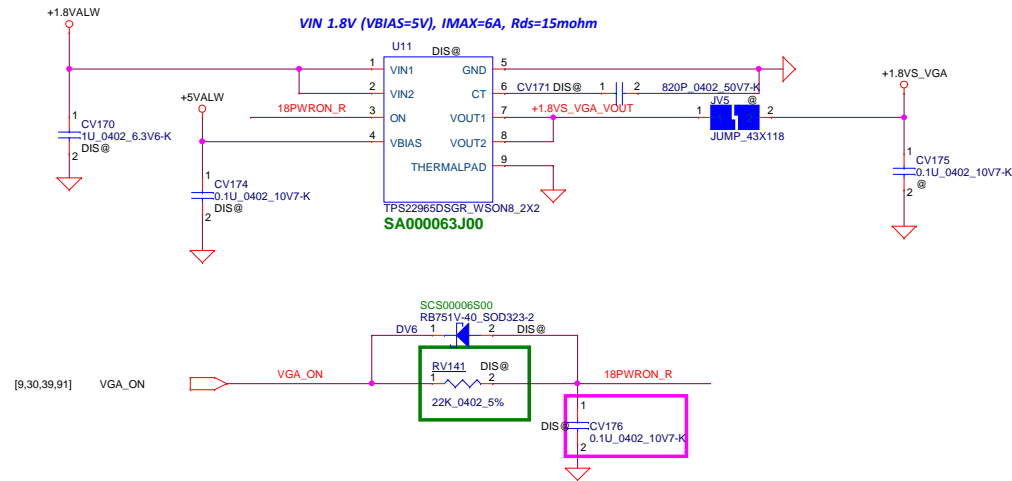
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								Date: Friday, October 23, 2015		Sheet 37 of 99 Rev 0.1

+1.5VS to +1.5VS_VGA

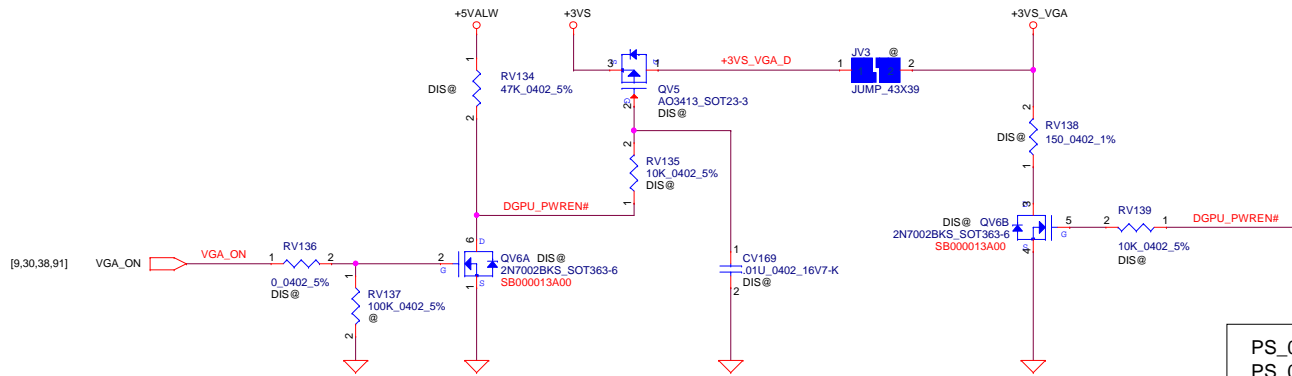


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+1.8VALW to +1.8VS_VGA

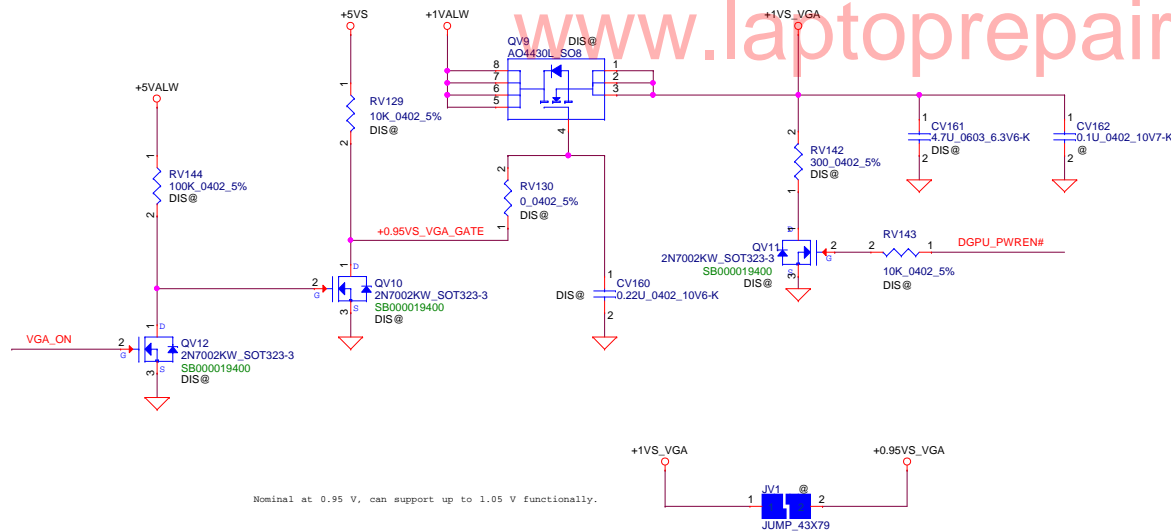


+3VS to +3VS_VGA




MLPS	Bit				
	5	4	3	2	1
PS_0[5:1]	1	1	0	0	1
PS_1[5:1]	1	1	0	0	0
PS_2[5:1]	1	1	0	0	0
PS_3[5:1]	1	1	X	X	X

+1VALW to +1VS_VGA




PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	STRAP_BIOS_ROM_EN = 1 ROM_CONFIG[2:0] = [001] 256MB
PS_0[4]	N/A	1 (Default)
PS_0[5]	N/A	1 (Default)
PS_1[1]	STRAP_BIF_GEN3_EN_A	0 = PCIe GEN3 is not supported
PS_1[2] PS_1[3]	STRAP_BIF_CLK_PM_EN N/A	0 = The CLKREQB power management capability is disabled 0 (Default)
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	1 = The transmitter full-swing is enabled
PS_1[5]	STRAP_TX_DEEMPH_EN	1 = Tx deemphasis enabled
PS_2[1]	N/A	0 (Default)
PS_2[2]	N/A	0 (Default)
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device
PS_2[4]	N/A	1 (Default)
PS_2[5]	N/A	1 (Default)
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	PS_3[3..1] 101 = Micron 2G 110 = Samsung 2G 111 = Hynix 2G
PS_3[4]	N/A	1 (Default)
PS_3[5]	N/A	1 (Default)


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				Date:	Friday, October 23, 2015	Sheet 40 of 99


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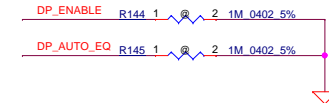
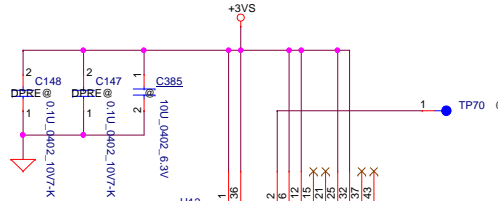
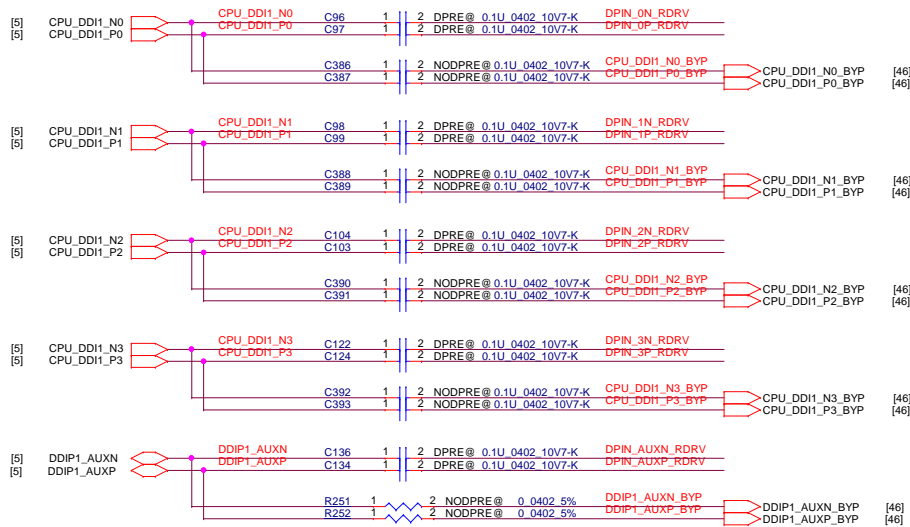
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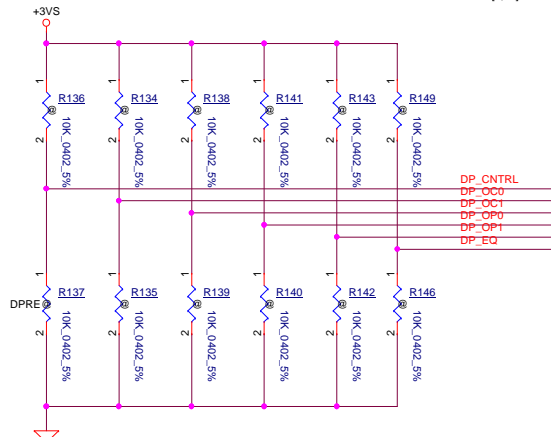
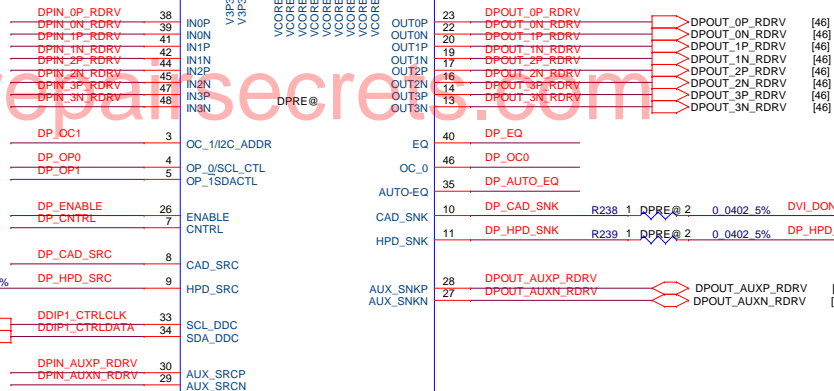
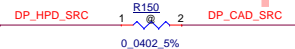
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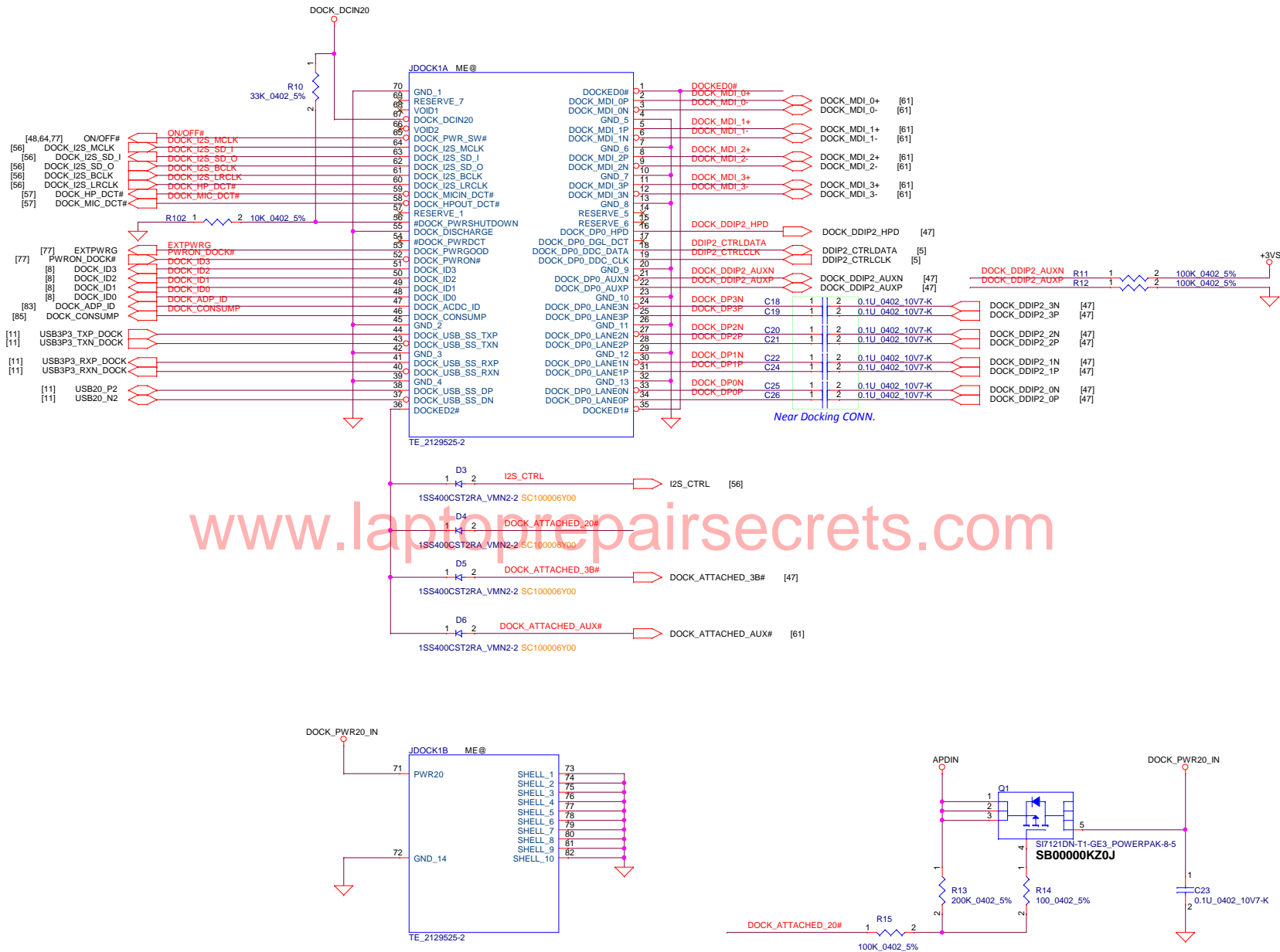
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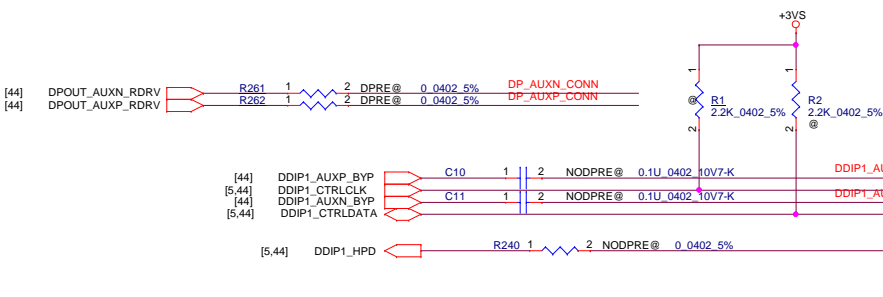


Follow mini DP SA0005W100 U1 design

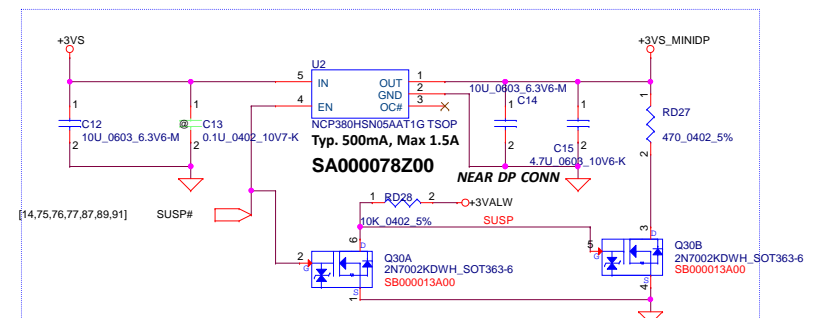
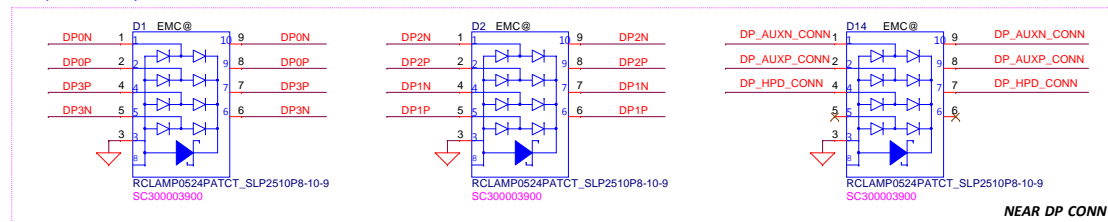
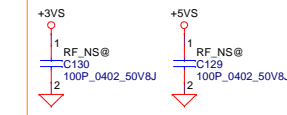



CNTRL	CAD_SNK	
0	0	Normal Mode for AUX
0	1	Normal Mode for DDC
1	X	Test Mode



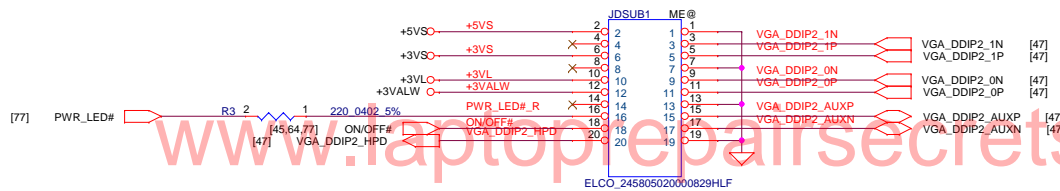


Reserve capacitor for LTE noise 2014.5.21

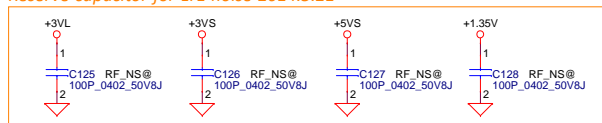


Title			
MINI-DP CONN.			
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M/B TO D-SUB/B BTB CONN.





Reserve capacitor for LTE noise 2014.5.21




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Title		Rev	
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Size	Document Number	BL460_NW-A651	
Custom			
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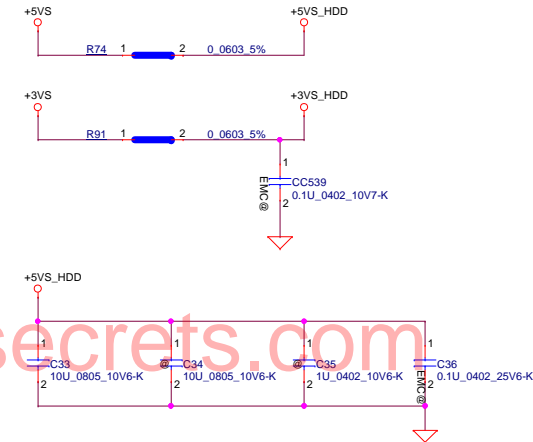
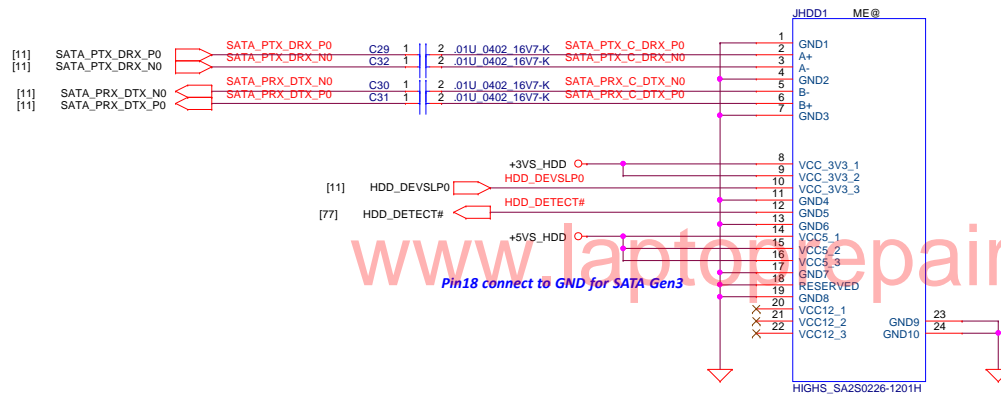
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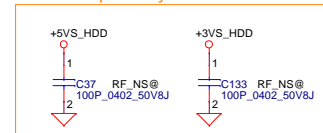
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SATA HDD CONN.



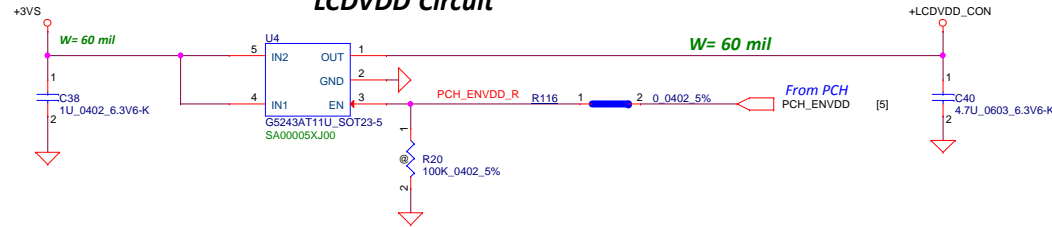
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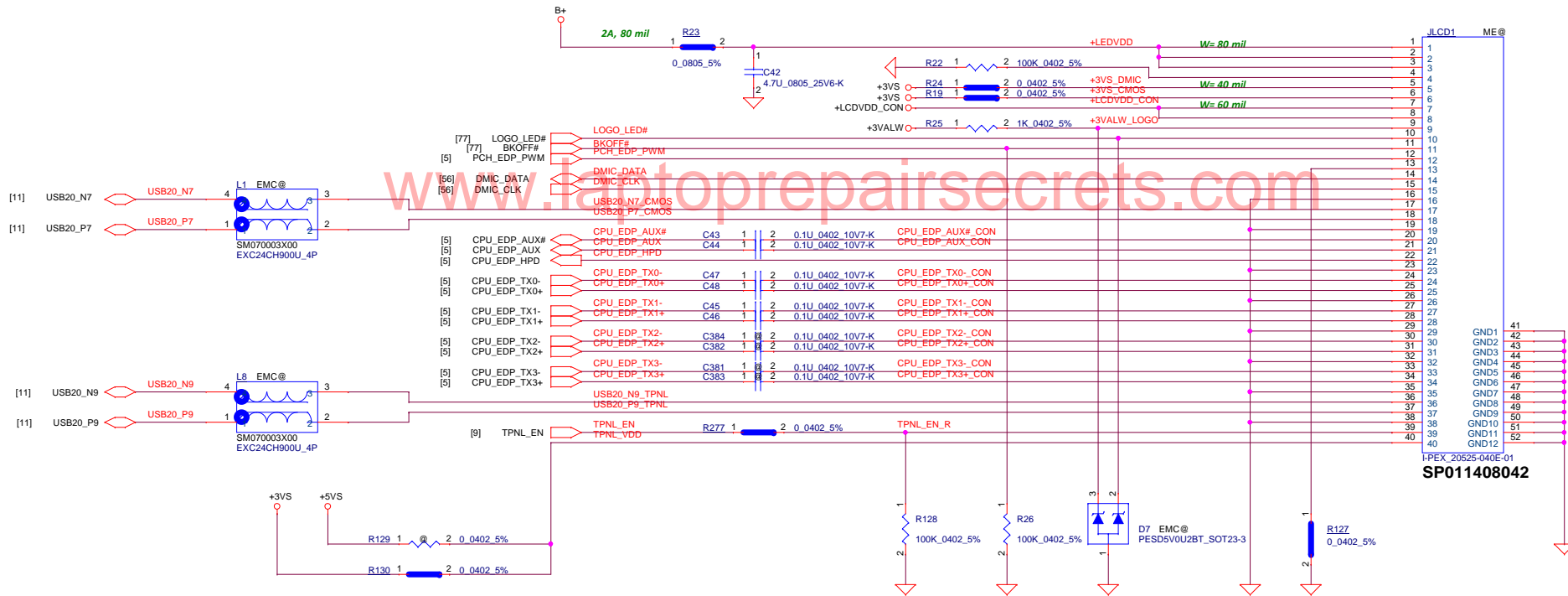
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Size	Document Number	Rev	0.1
Custom	BLA60_NW-A651		
Date:	Friday, October 23, 2015	Sheet	51 of 99

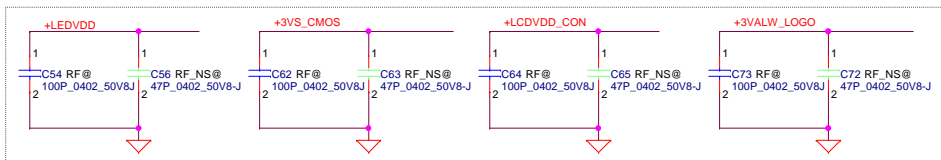
LCDVDD Circuit



eDP/CMOS/LOGO-LED CONN.



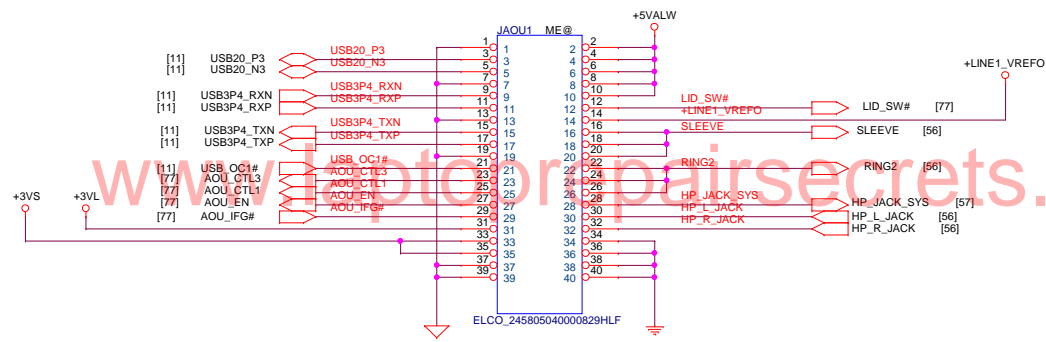
RF



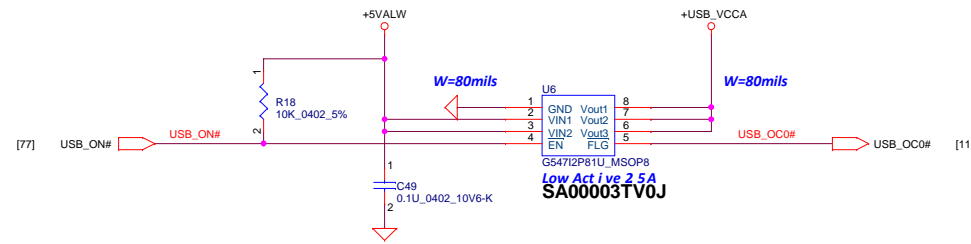
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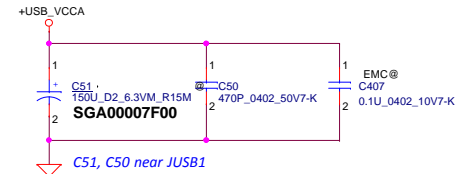
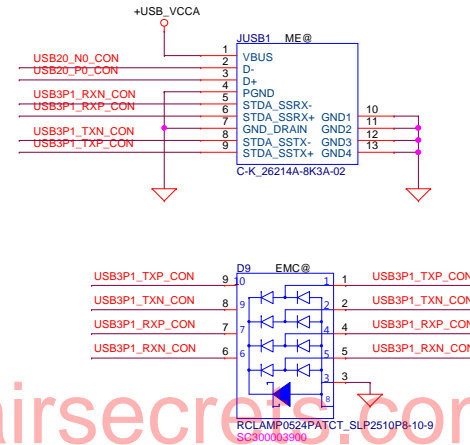
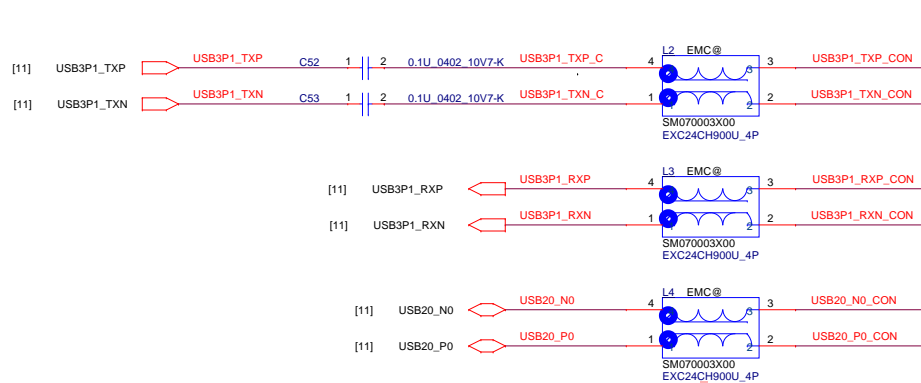
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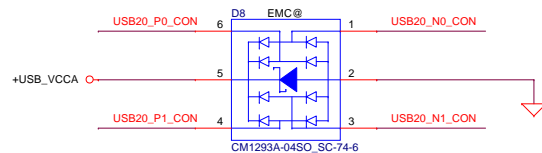
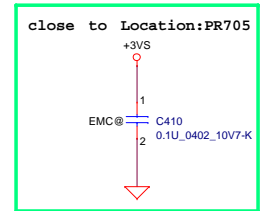
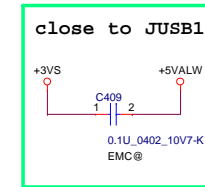
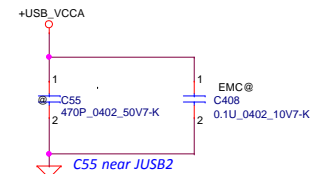
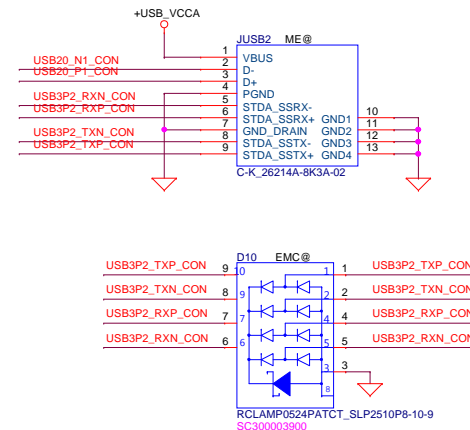
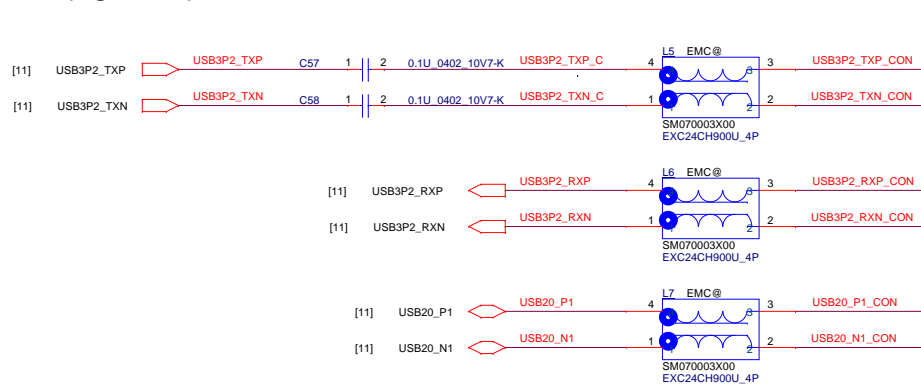
USB POWER SWITCH




On Board (Right-Front)




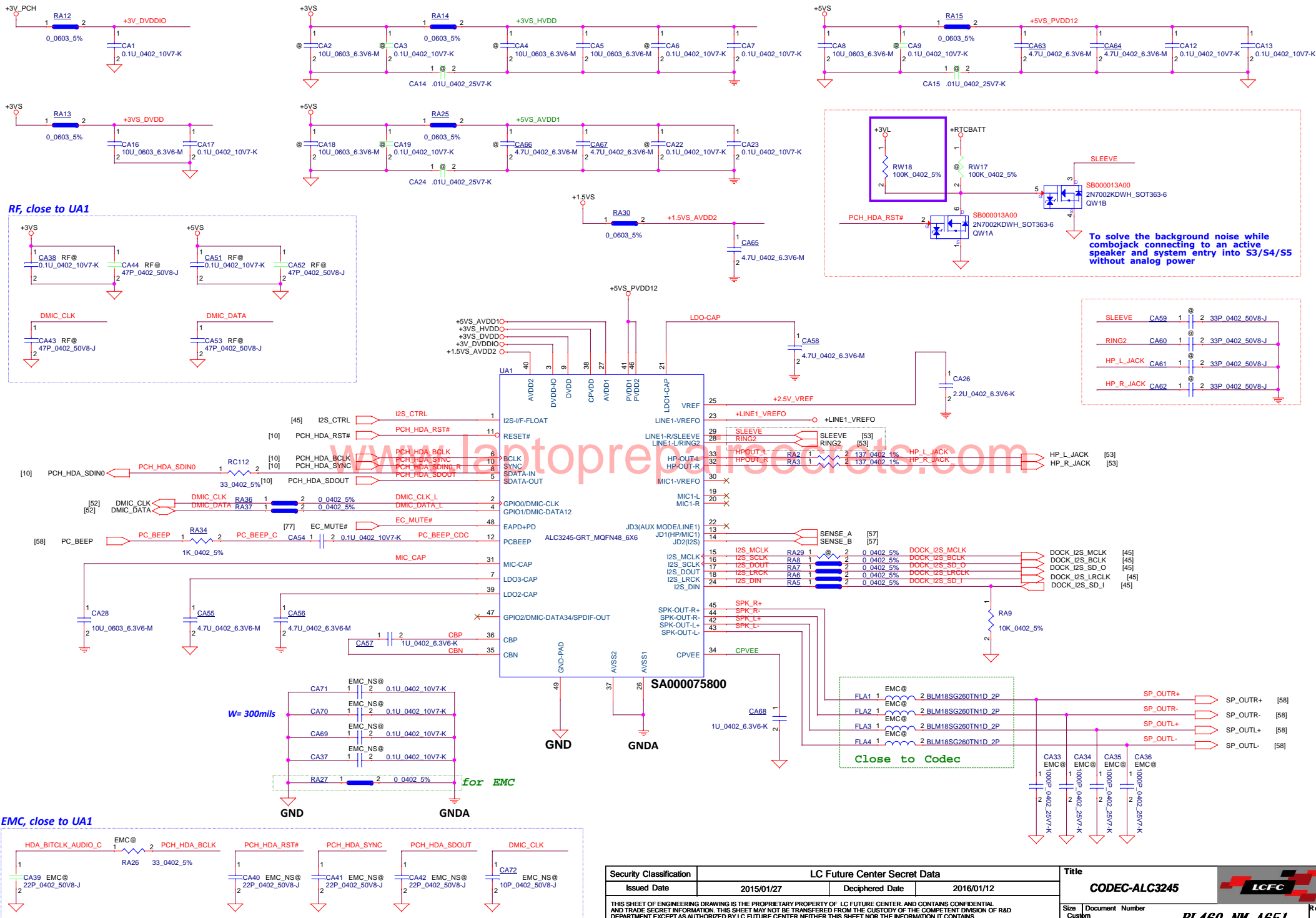
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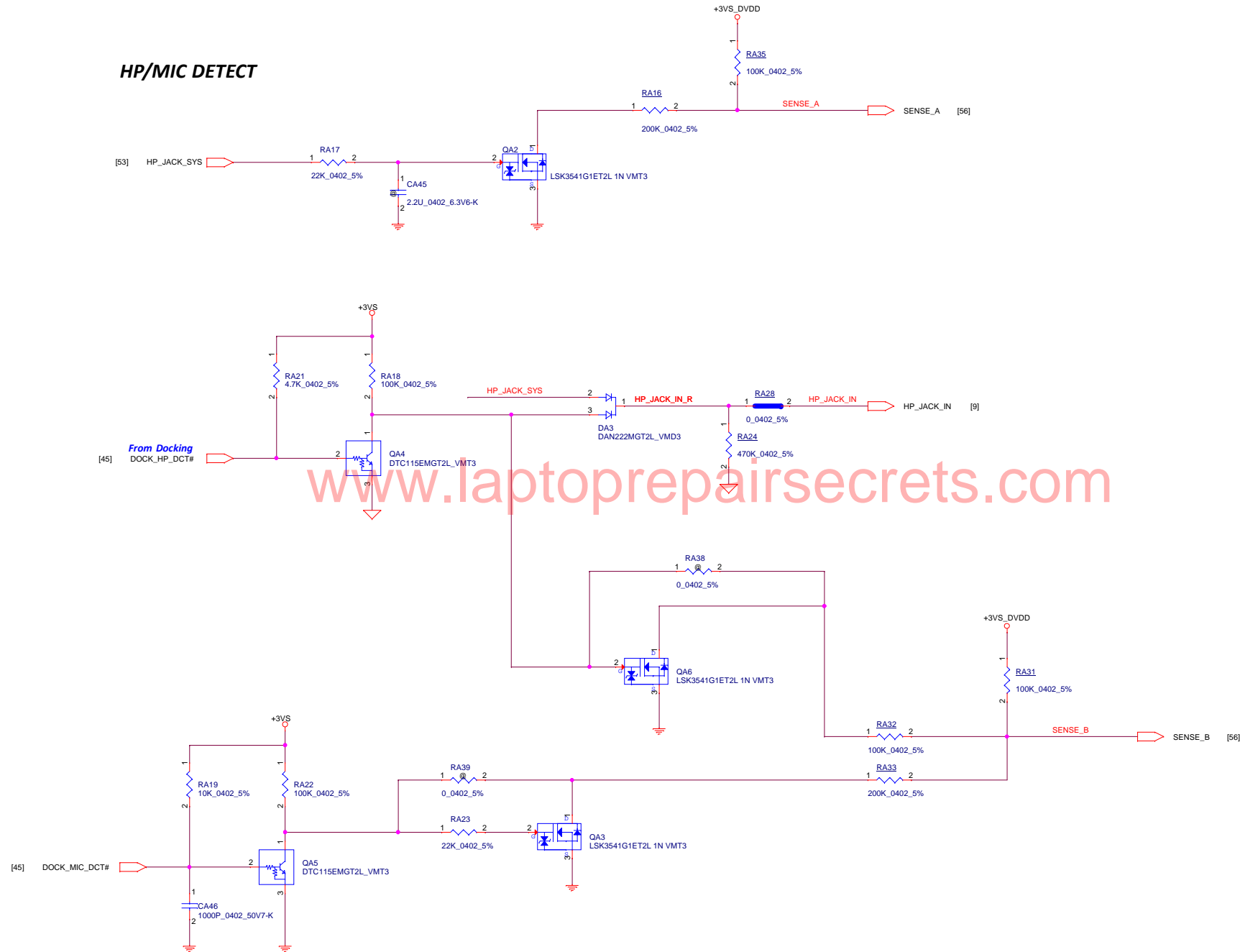
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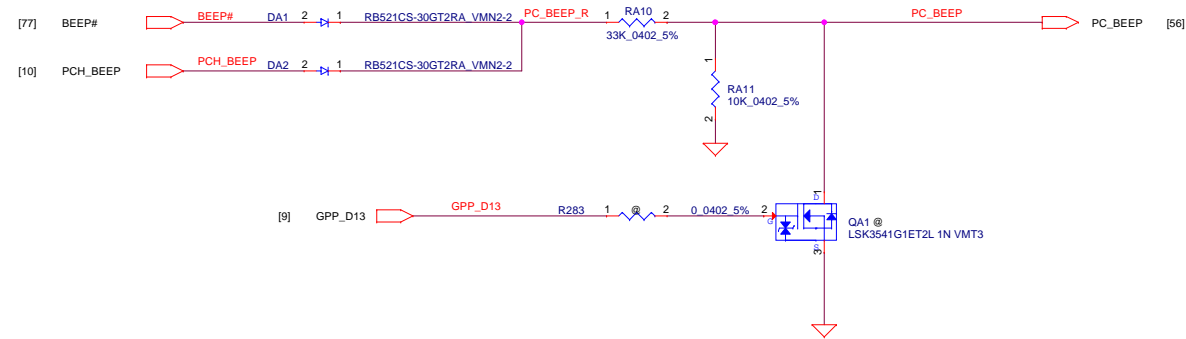


HP/MIC DETECT



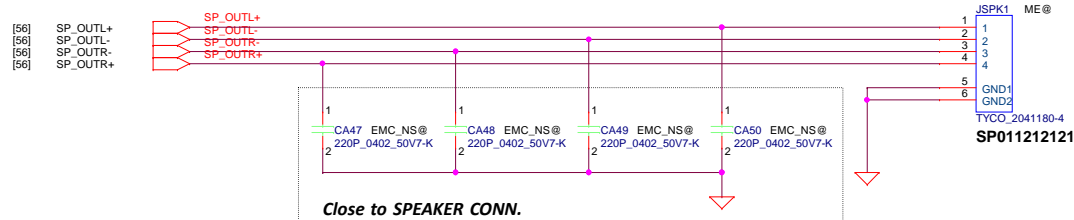
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Issued Date	2015/01/12	Deciphered Date	2016/01/12	HP/MIC DETECT		
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				Sheet	57 of 99	

PC-BEEP




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SPEAKER CONN.

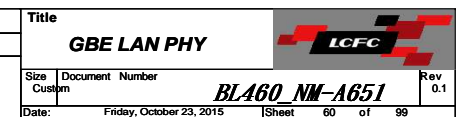


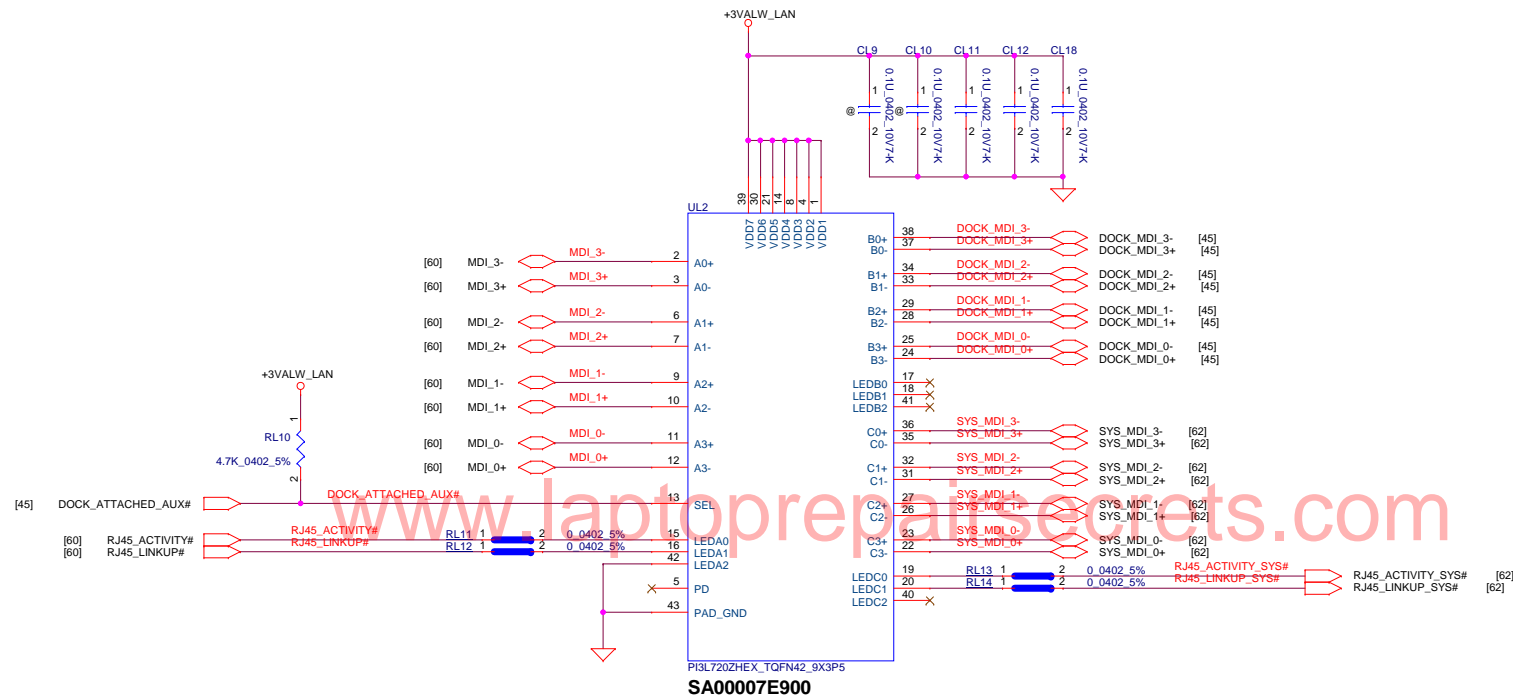
Close to SPEAKER CONN.

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Custom						0.1
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				Date:	Friday, October 23, 2015	Sheet 59 of 99



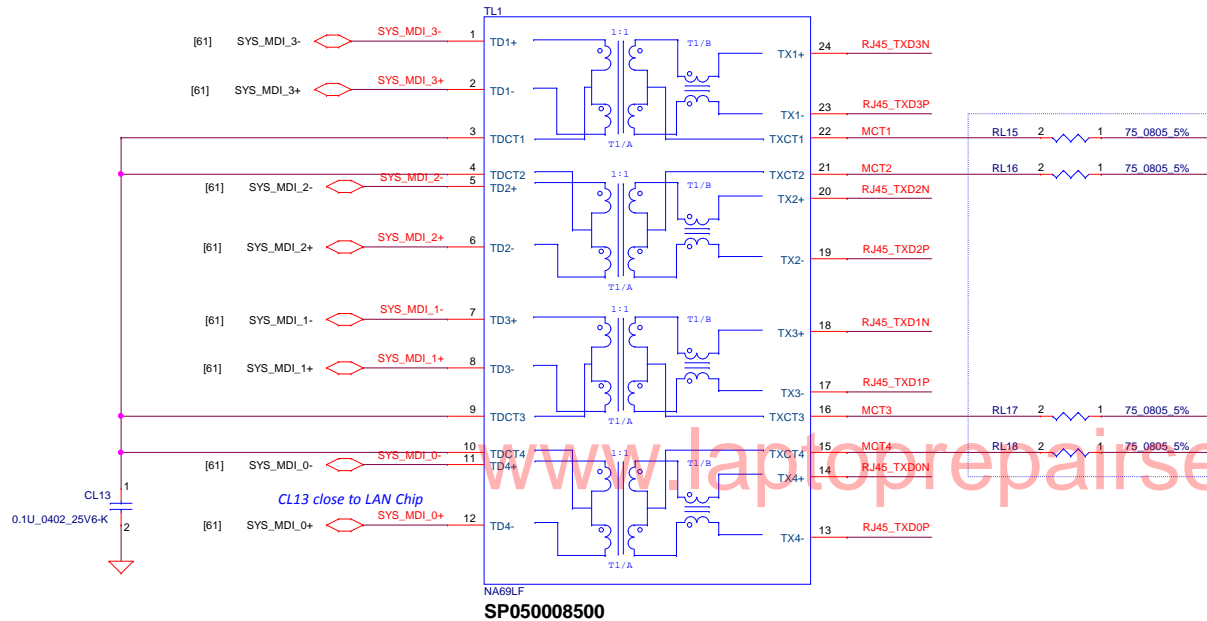


Vendor	P/N	NOTE
Pericom	PI3L720ZHE+CX, SA00007E900	Main Source
ONsemi	NCN7201, SA00005TF00	2nd Source (FVT)

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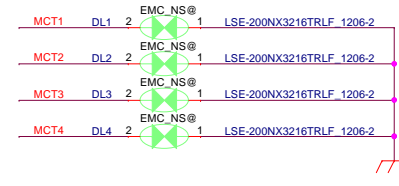
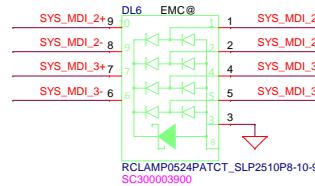
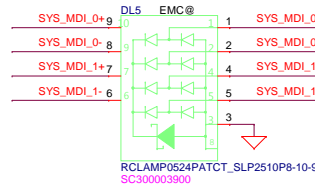
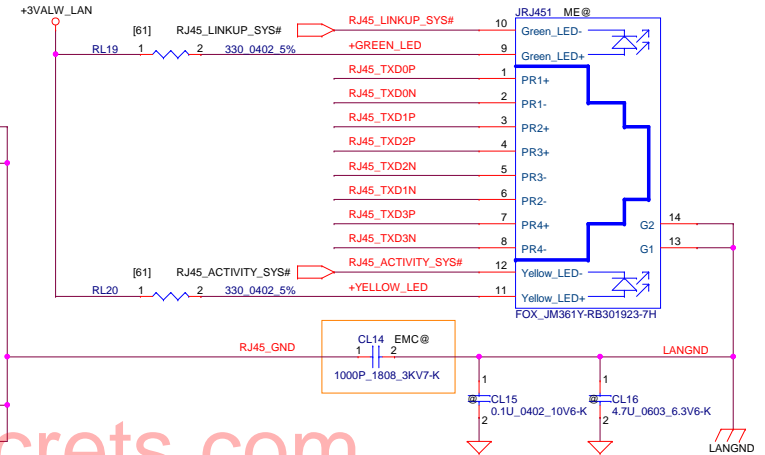
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Size Custom	Document Number	BLA60_NW-A651		Rev 0.1
Date:	Friday, October 23, 2015	ISheet	61 of 99	


LAN X' FORM



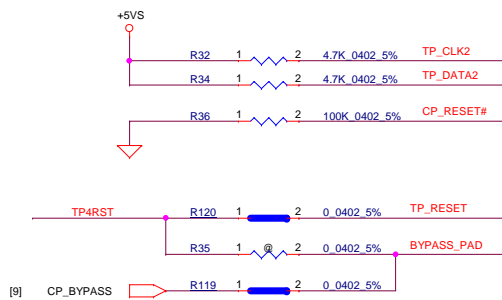
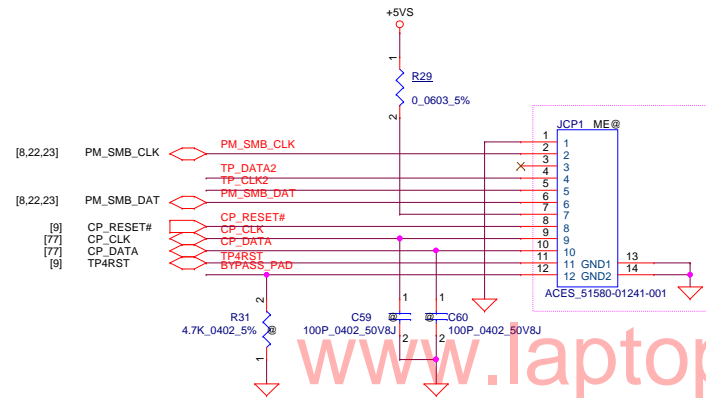
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RJ45 Conn.

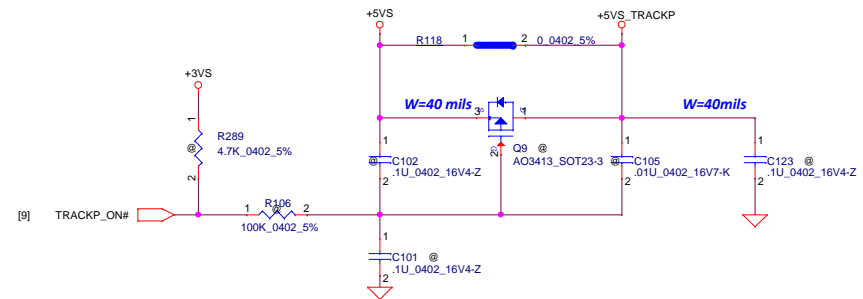
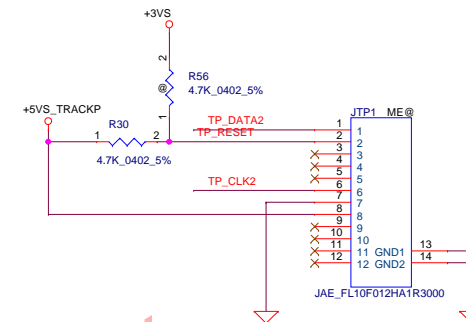


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Custom						0.1
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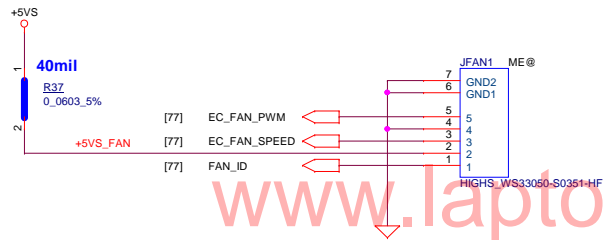
5-Button Click Pad



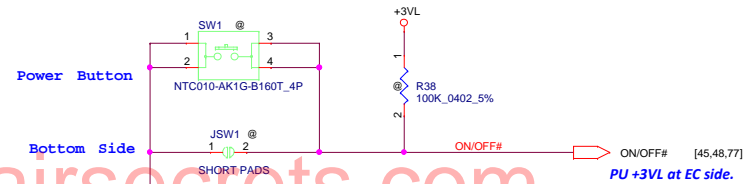
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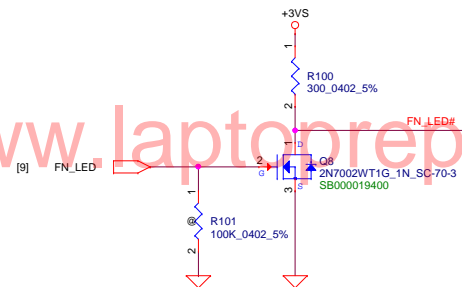
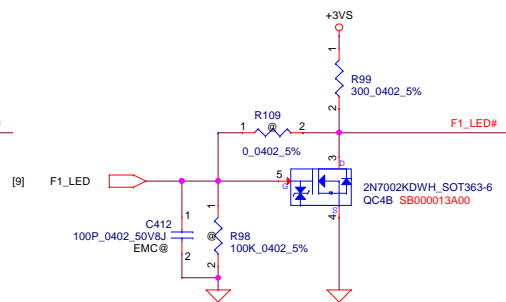
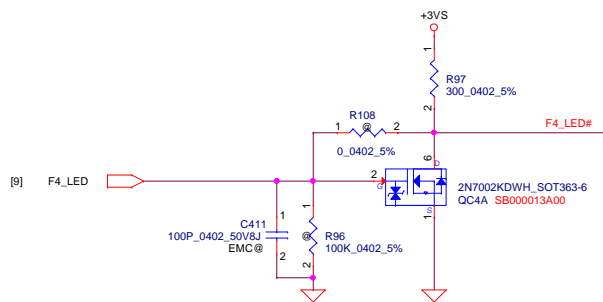


FAN CONN.



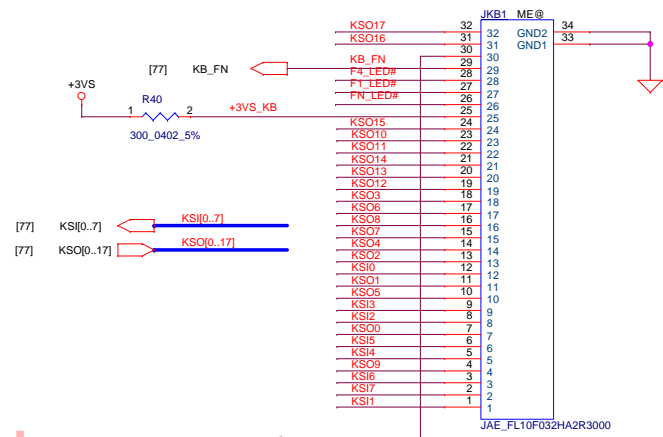
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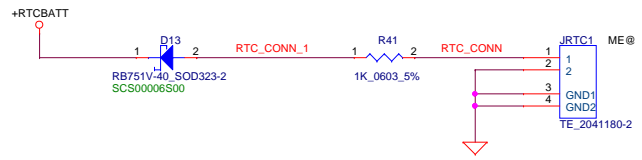


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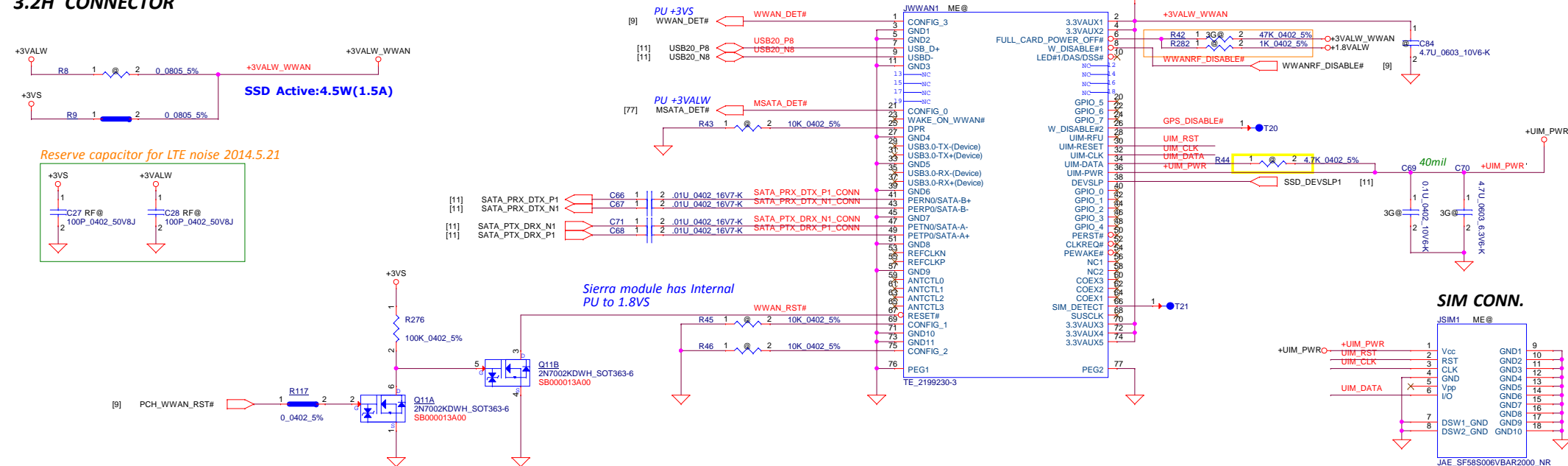
KB CONN



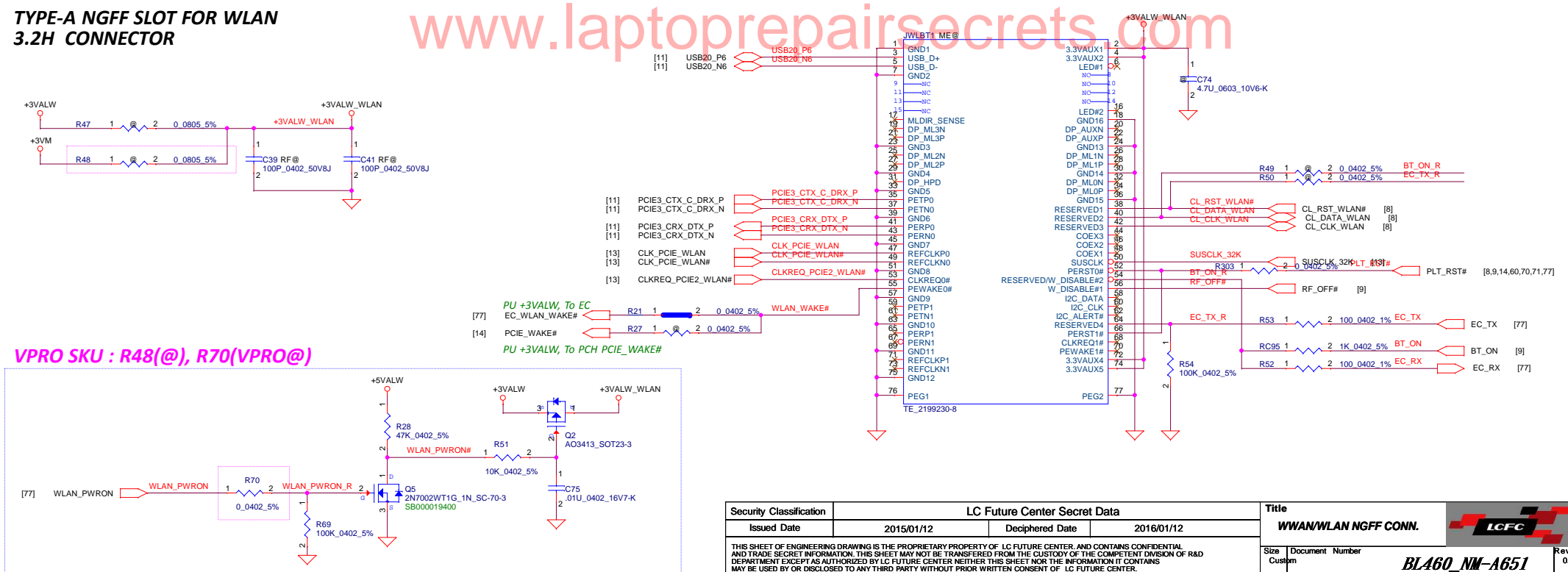
RTC CONN.




TYPE-B NGFF SLOT FOR WWAN/SSD 3.2H CONNECTOR




TYPE-A NGFF SLOT FOR WLAN 3.2H CONNECTOR




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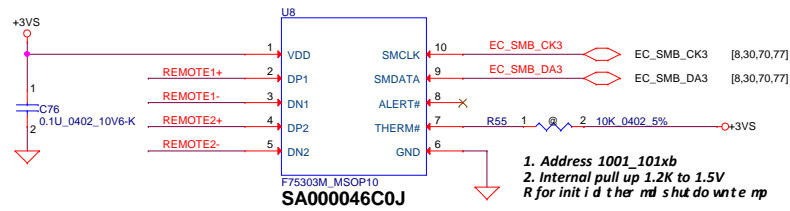
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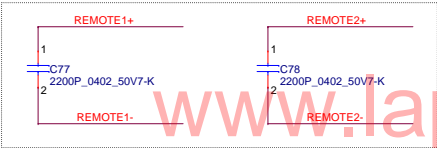
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				Date:	Friday, October 23, 2015	Sheet	68 of 99
						BL460 NW-A651	

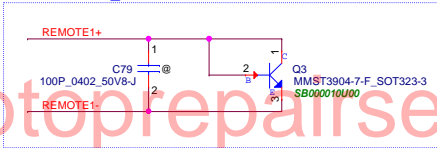
Thermal Sensor



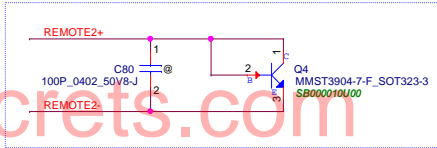
Close to U8



Close to +VCC_CORE

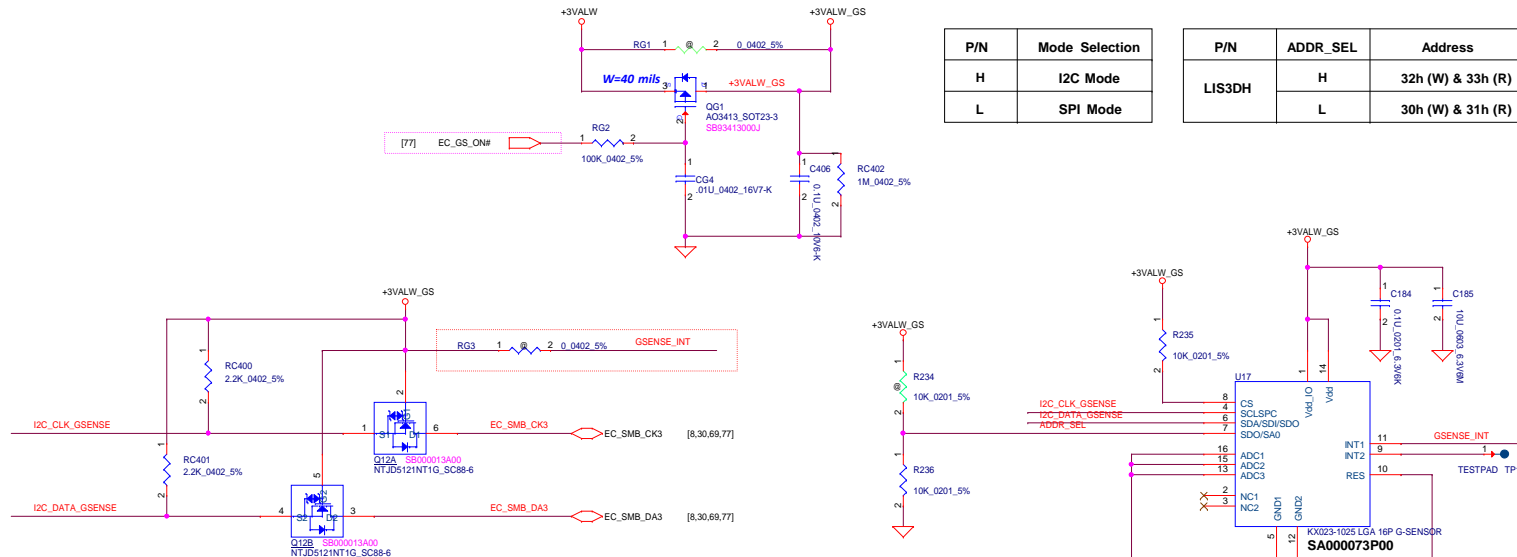


Close JDIMM1&JDIMM2



REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

APS G-Sensor



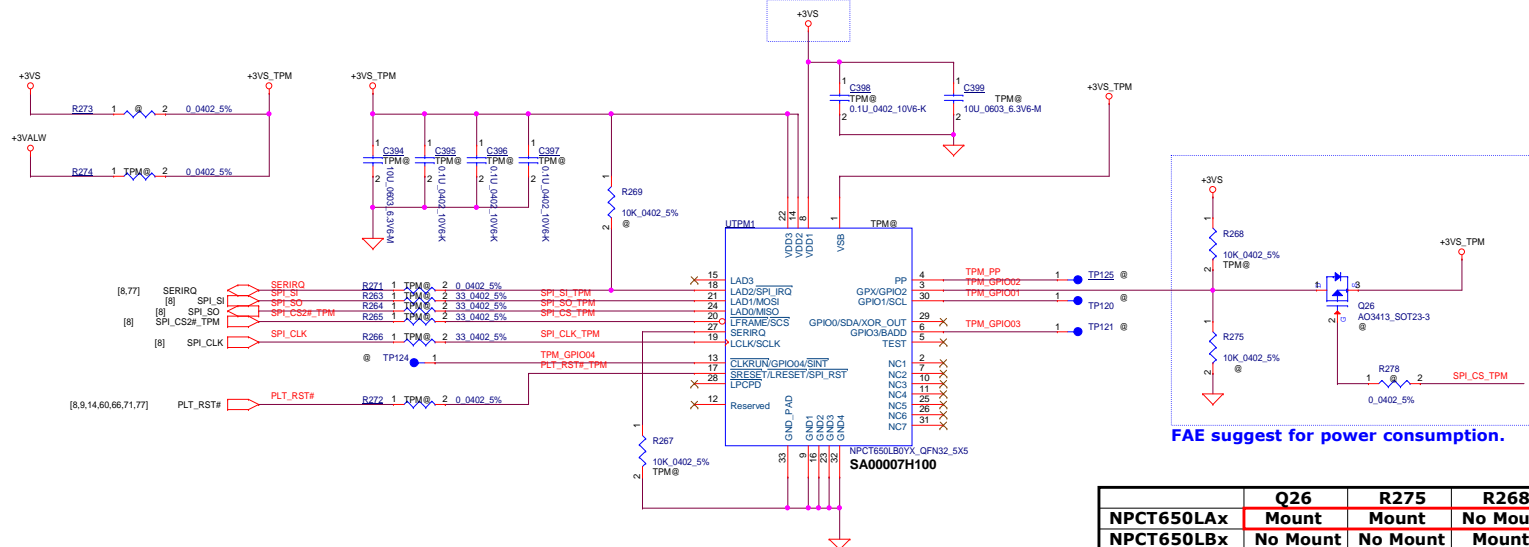
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H	I2C Mode
L	SPI Mode

P/N	ADDR_SEL	Address
LIS3DH	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)

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TPM IC


FAE suggest for power consumption.

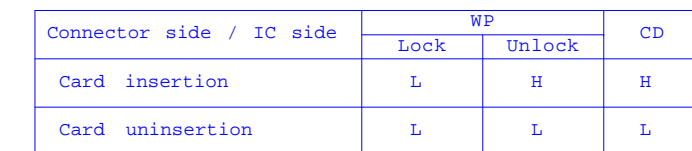
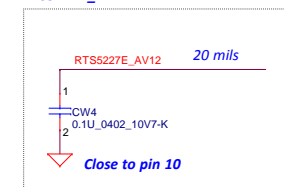
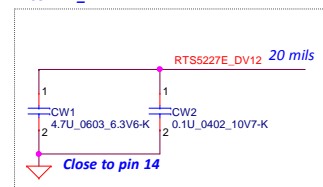
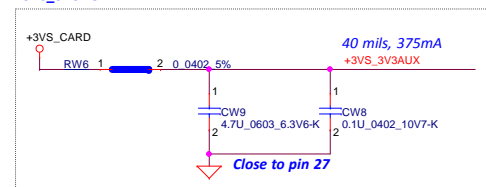
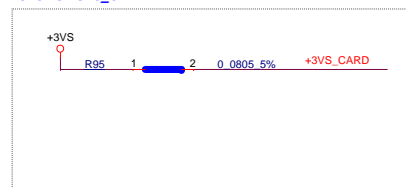



FAE suggest for power consumption.

	Q26	R275	R268
NPCT650LAx	Mount	Mount	No Mount
NPCT650LBx	No Mount	No Mount	Mount


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Title			Rev 0.1
G SENSOR / TPM			
Size C	Document Number	BL460 NM-A651	
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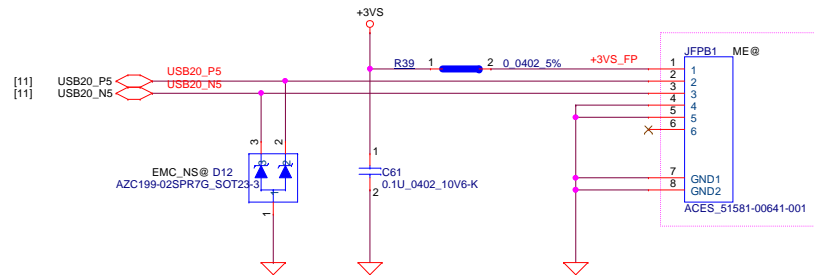


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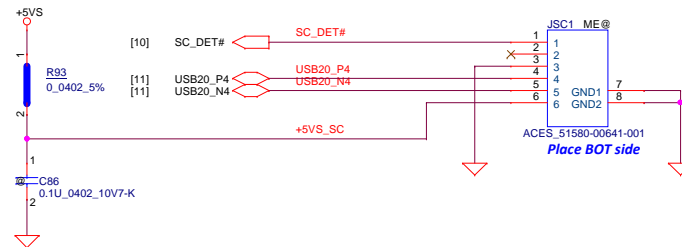
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FingerPrint CONN.




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SMART CARD CONN.

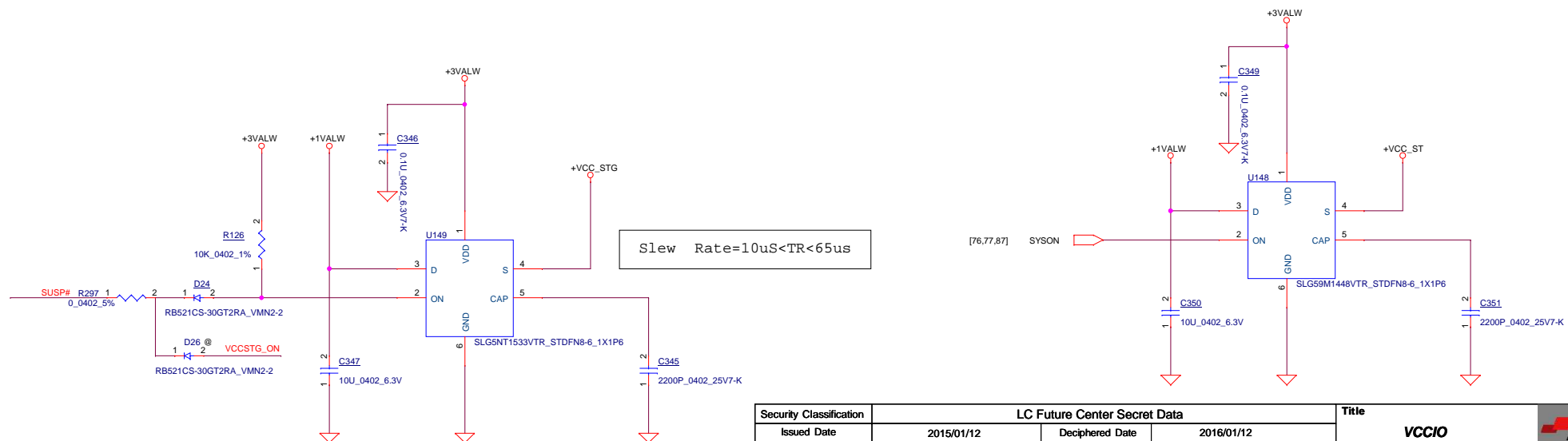
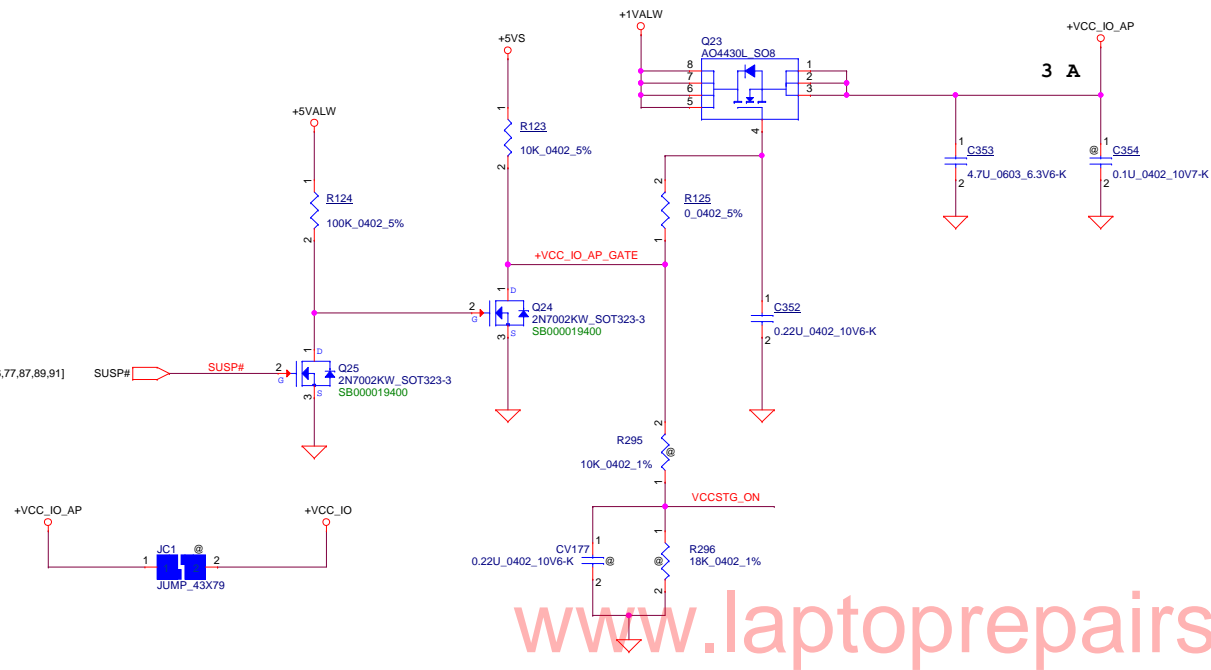



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				BL460 NM-A651
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				Date: Friday, October 23, 2015 Sheet 73 of 99

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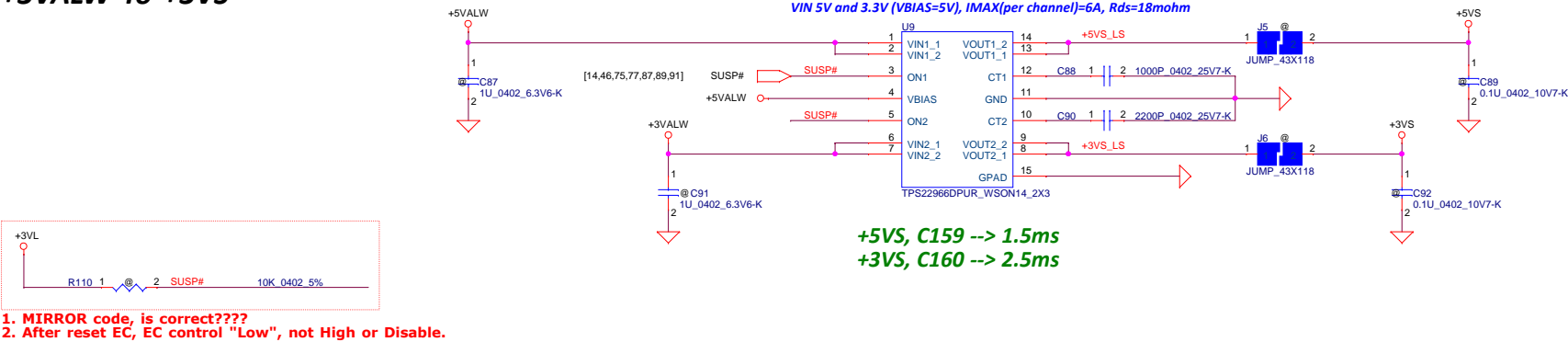
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				Custom		0.1	
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+1VALW to +VCC_IO_AP

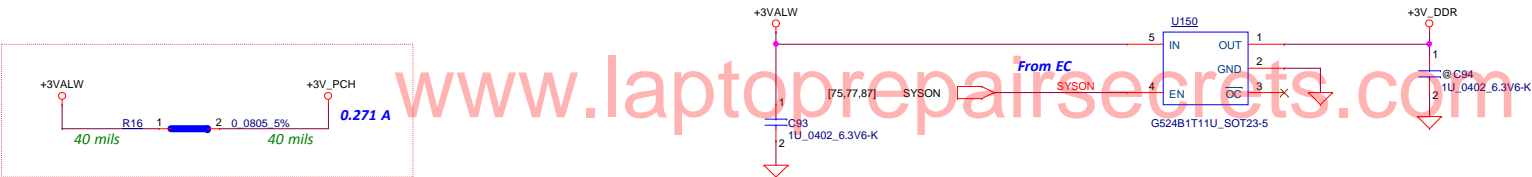


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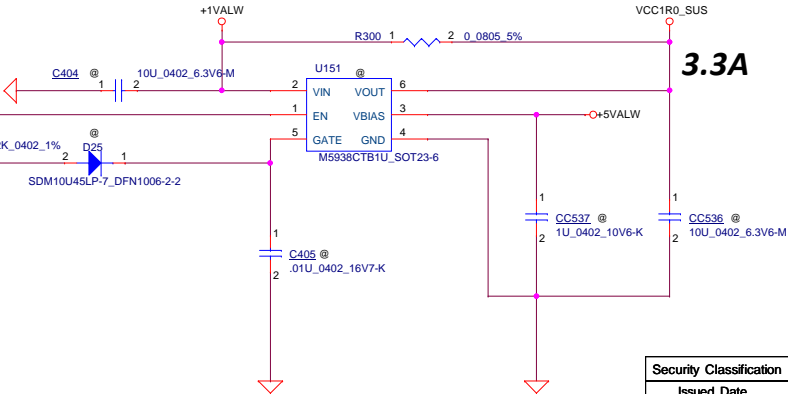
Smart Switch
+5VALW To +5VS
+3VALW To +3VS



+3VALW To +3V_PCH : Short, Don't support Deep Sx

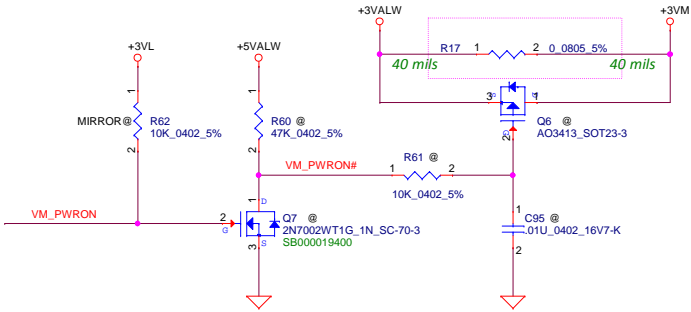



+1VALW to VCC1R0_SUS

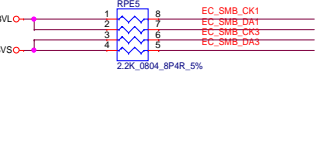
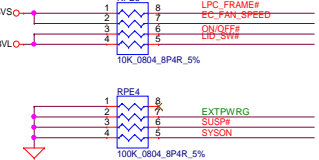
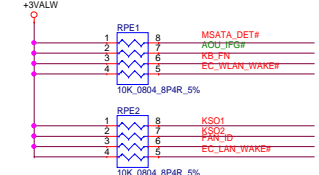
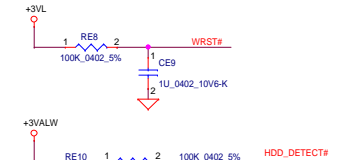
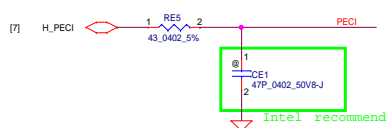


+3VALW to +3VM
VPRO : SPI ROM

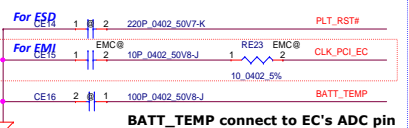
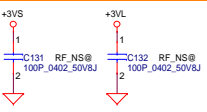
+3VM to SPI ROM.
Reserve for LAN and WLAN.



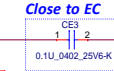
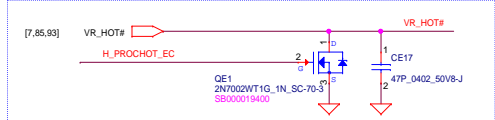
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						Size		Document Number		Rev	
						Custom		BL460_NW-A651		0.1	
						Date:		Friday, October 23, 2015		Sheet 76 of 99	



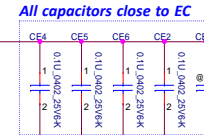
Reserve capacitor for LTE noise



PROCHOT#
(EC asserts PROCHOT# signal by driving high, the level shifter must invert it and drive the processor side PROCHOT# low.)



Close to EC



minimum trace width 12 mil

IT8586E/AX
LQFP-128L

EXTERNAL SERIAL FLASH

SPI Flash ROM

UART

GPIO

SM Bus

WAKE UP

GPIO

GPIO

GPIO

GPIO

GPIO

GPIO

GPIO

GPIO

GPIO

GPIO

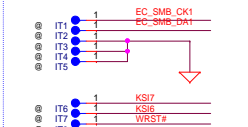
GPIO

GPIO

GPIO

GPIO

For factory EC flash



Security Classification

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Issued Date

2015/01/12

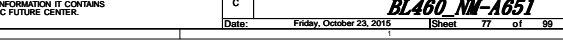
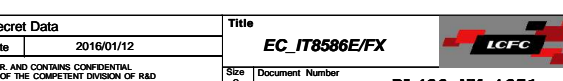
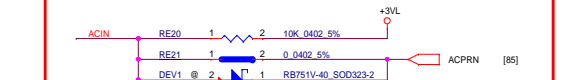
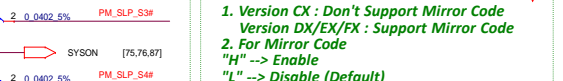
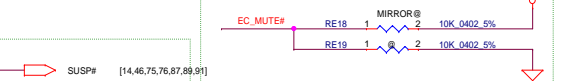
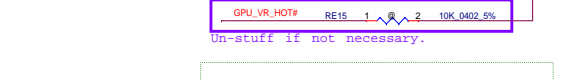
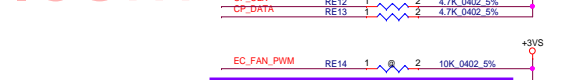
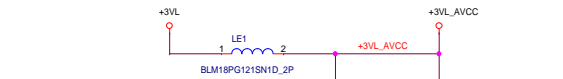
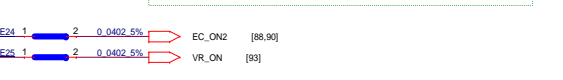
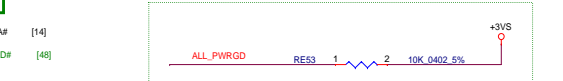
Deciphered Date

2016/01/12

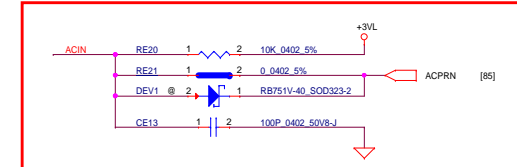
Vcc 3.3V +/- 5%

RE6 100K +/- 1%

Board ID	RE7	V _{AD_BID} min	V _{AD_BID} tYP	V _{AD_BID} max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	FVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	FVT2
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SIT
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	SIT-R
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	SVT



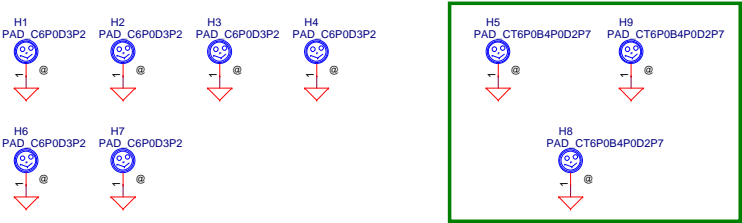
AC IN, need to confirm the pin is High or Low active while pulg ACIN



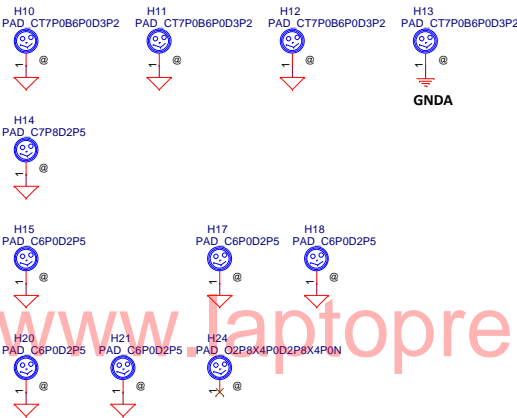
1. Version CX : Don't Support Mirror Code
2. Version DX/EX/FX : Support Mirror Code
3. For Mirror Code "H" --> Enable
4. "L" --> Disable (Default)

Screw Hole

For CPU and GPU



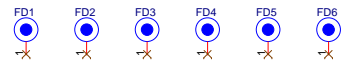
For ME GND hole





For ME hole




PCB Fedical Mark PAD




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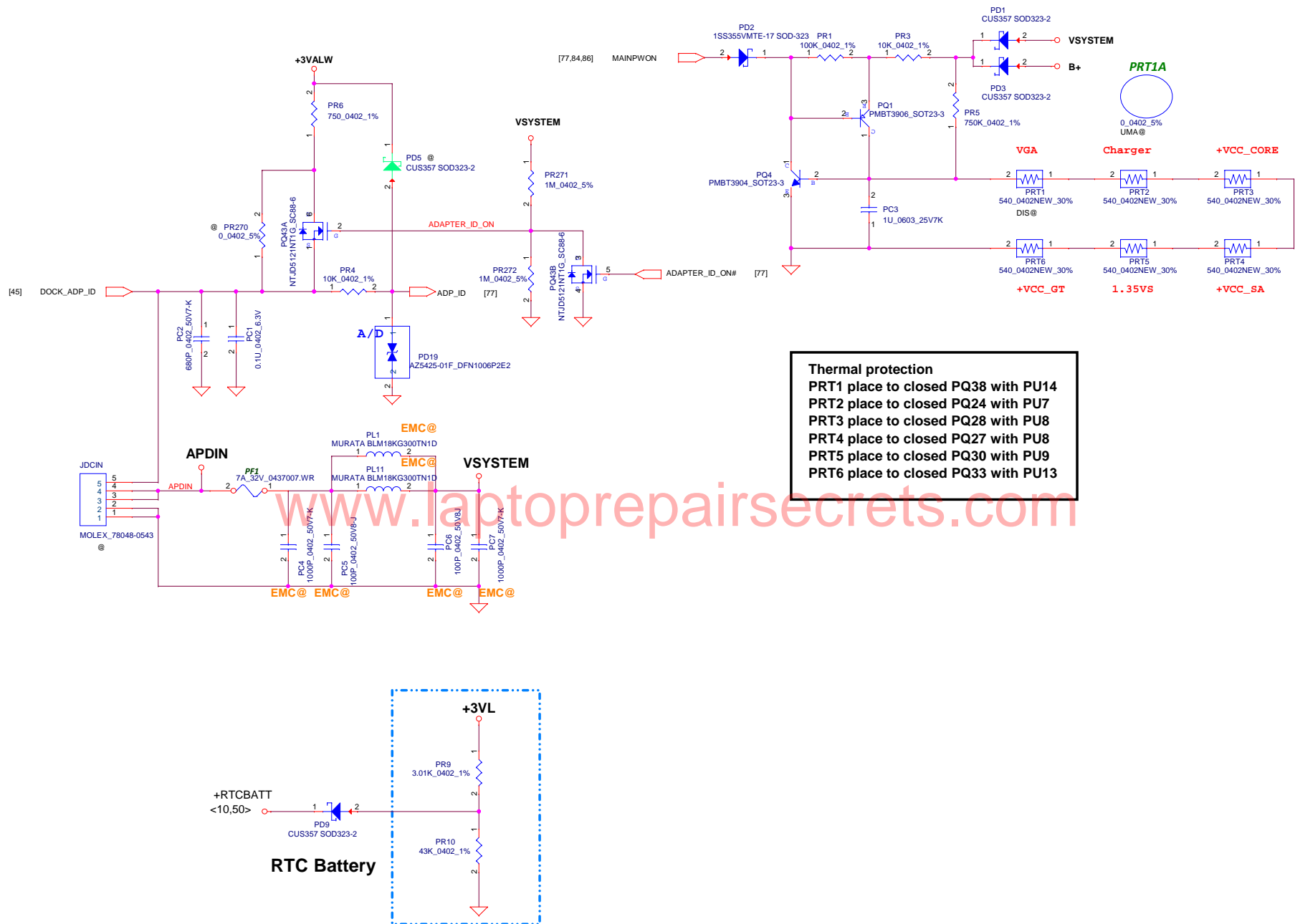
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+RTCBATT

<10,50>

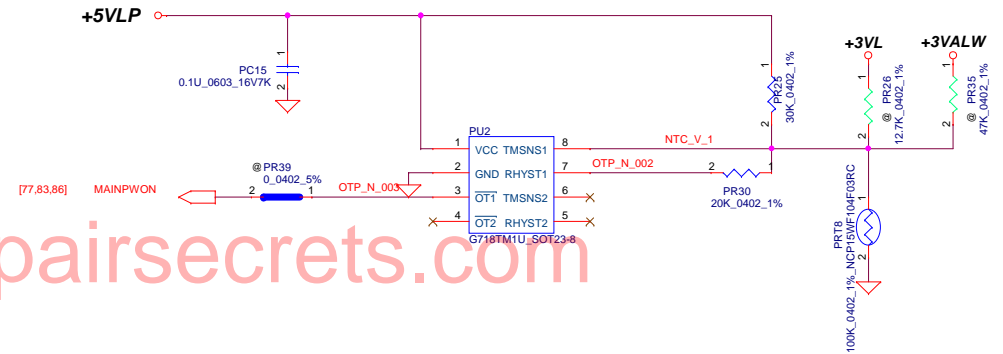
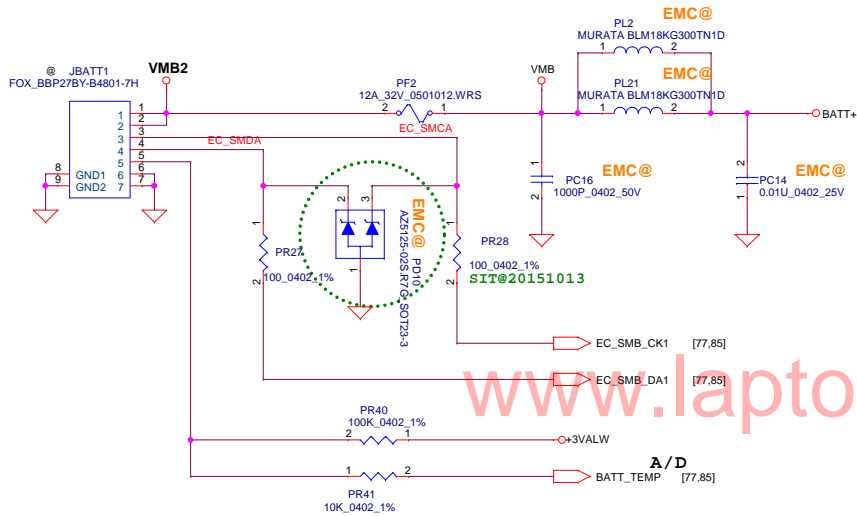
RTC Battery

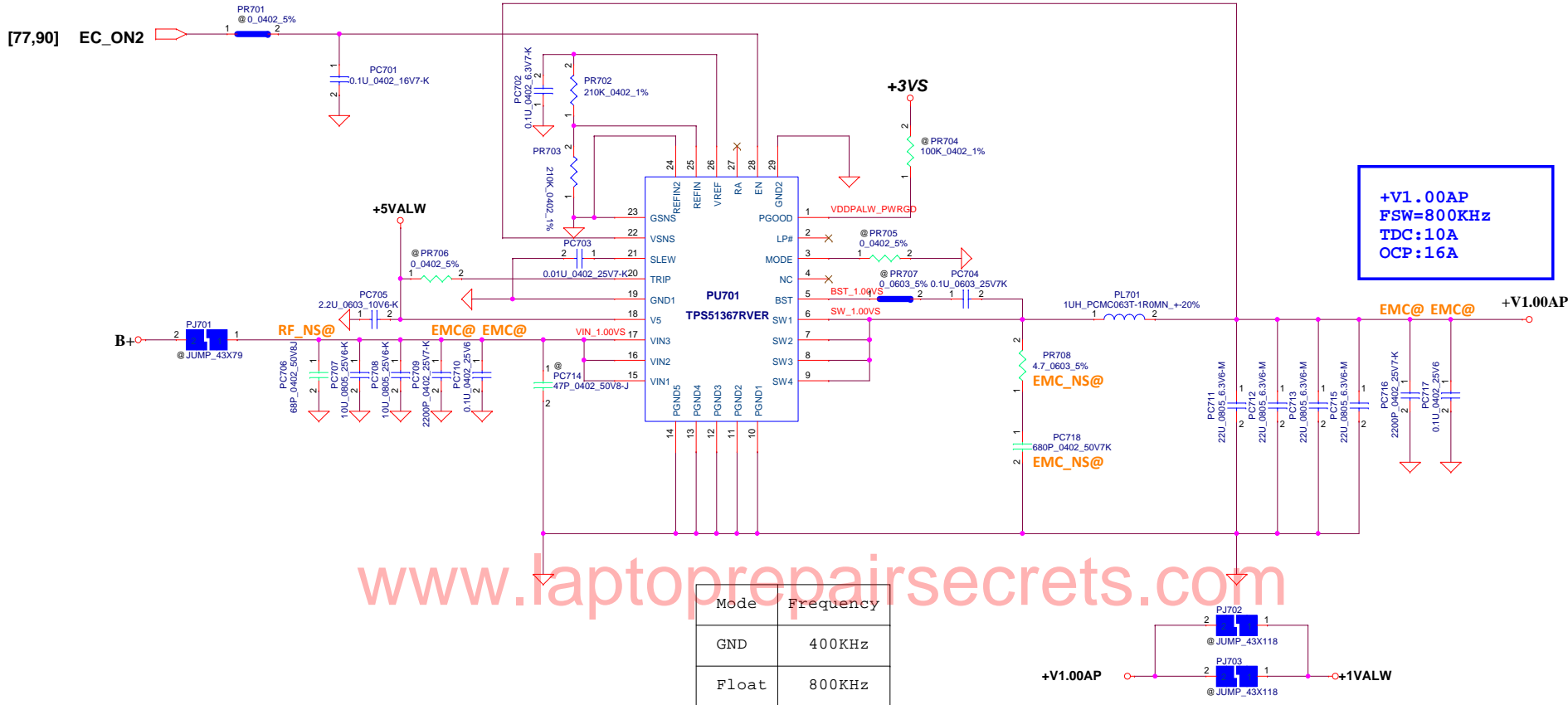
SDV20150525

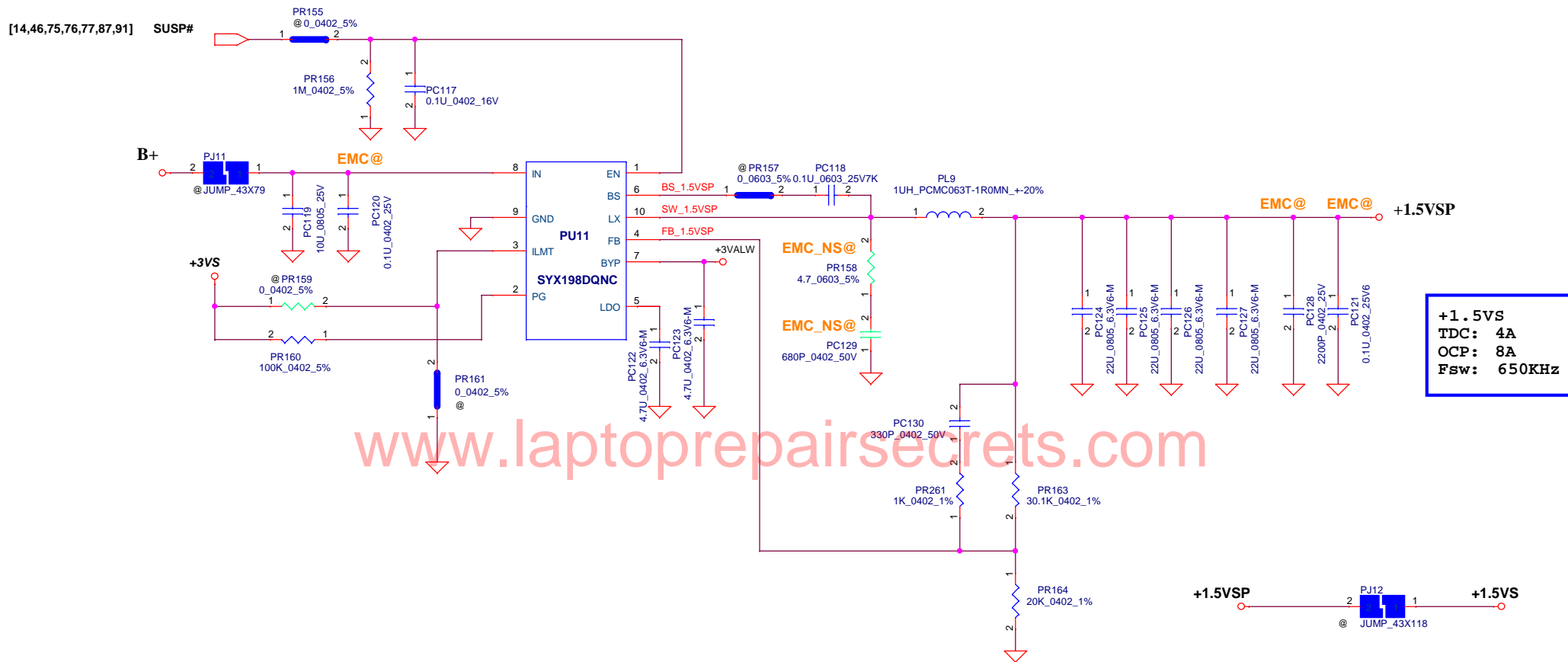
Follow EE suggestion to
modify RTC voltage circuit.


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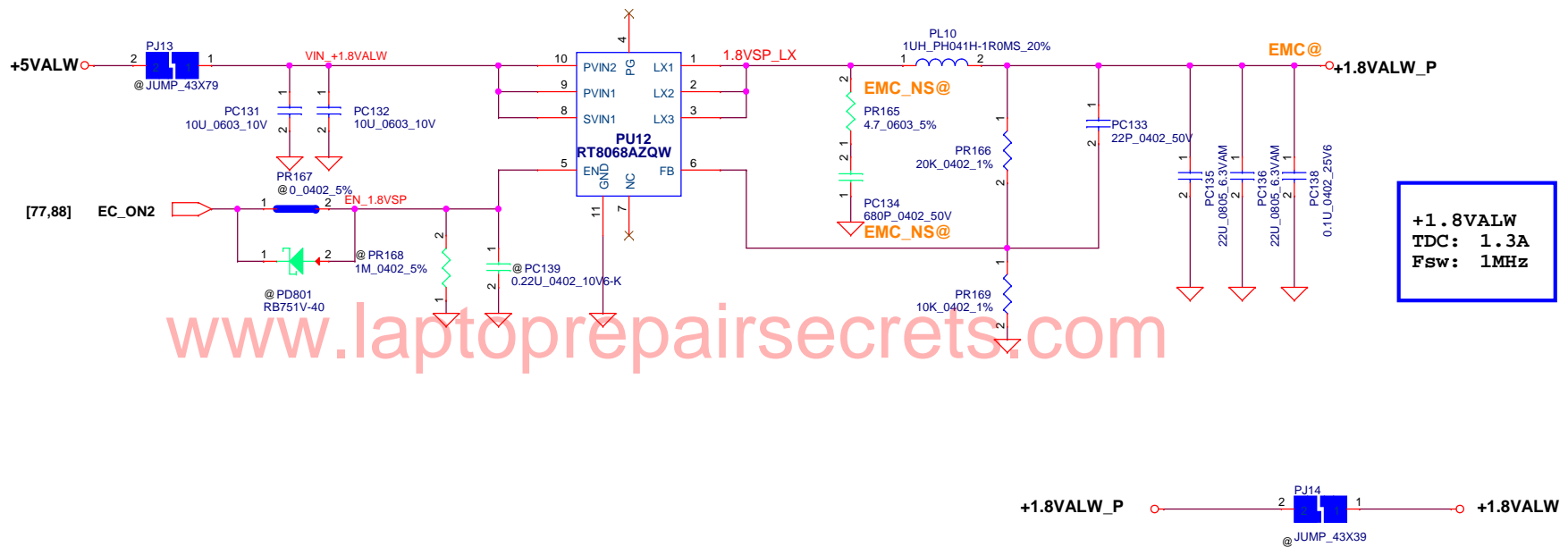
PRT8 under CPU botten side :
CPU thermal protection at 92 +-3 degree C
Recovery at 60 +-3 degree C




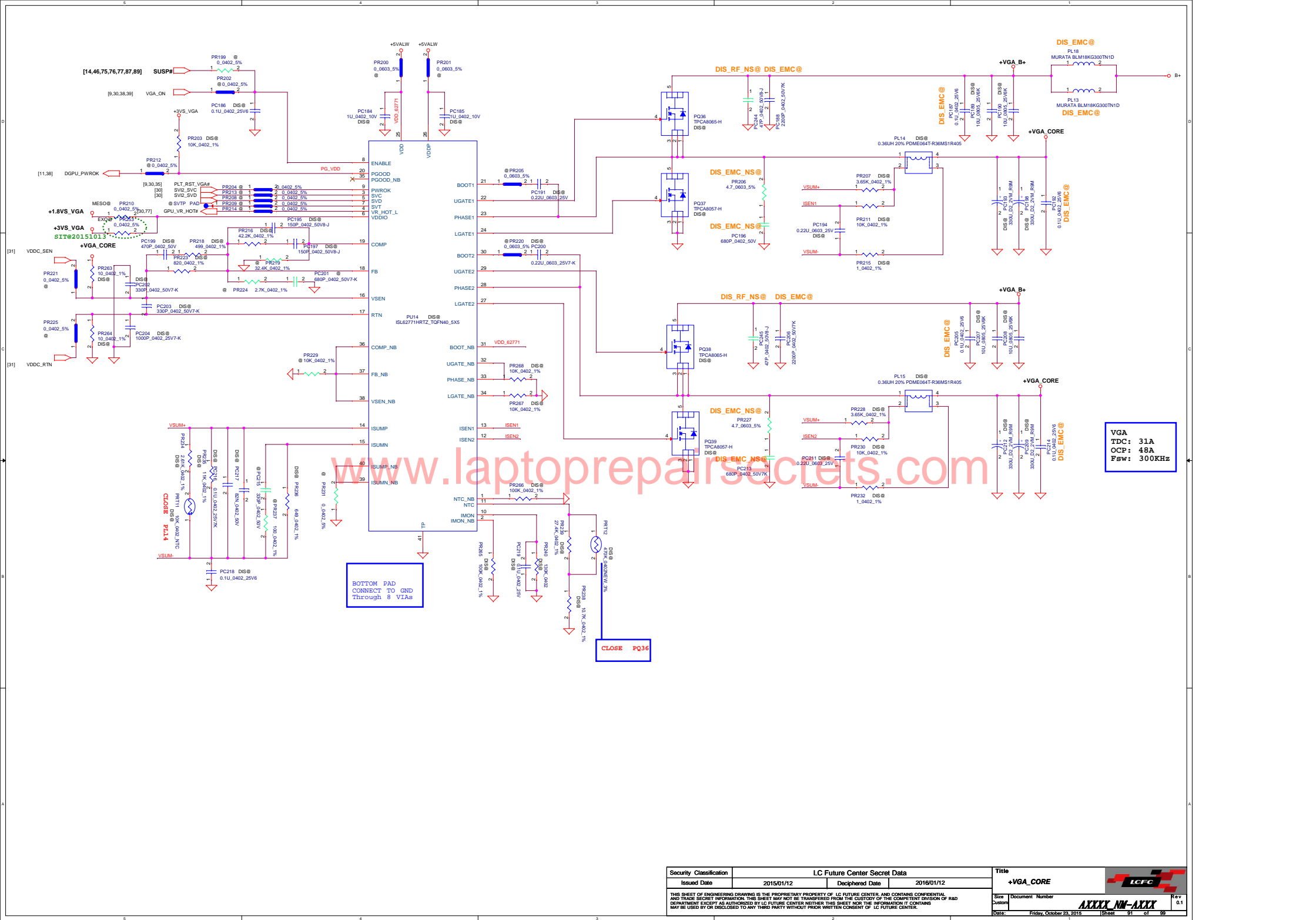





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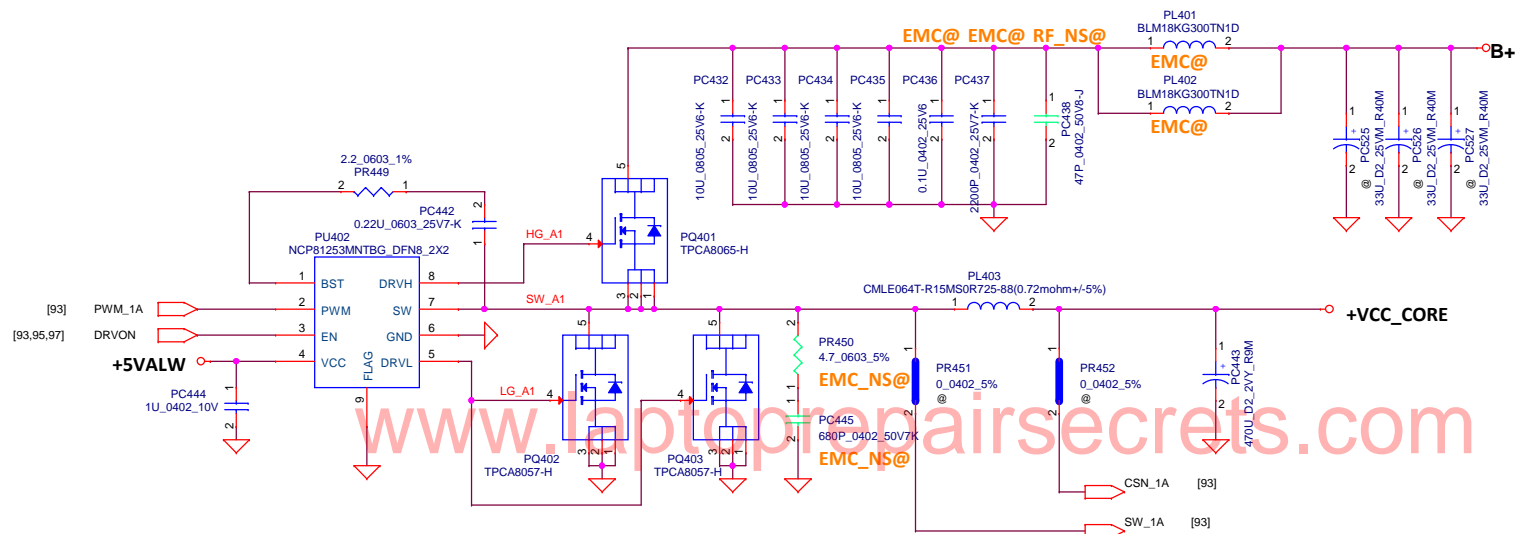
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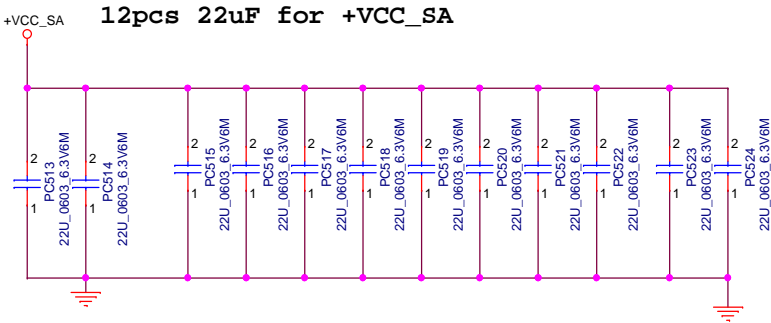
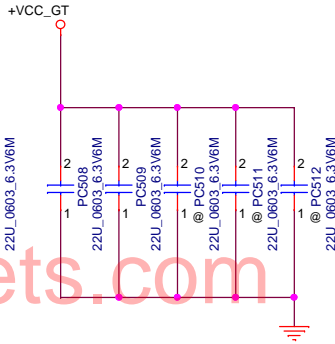
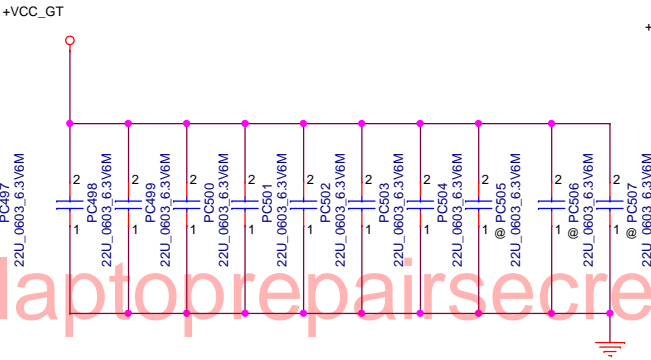
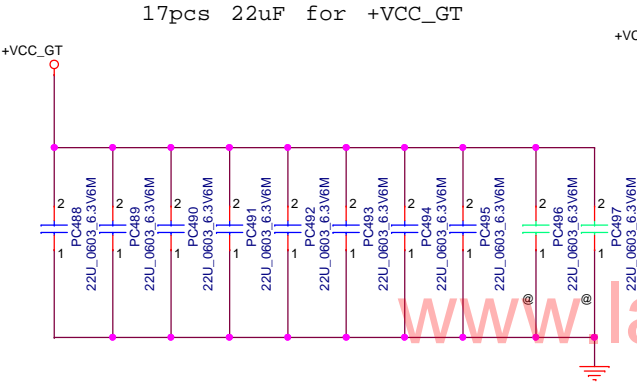
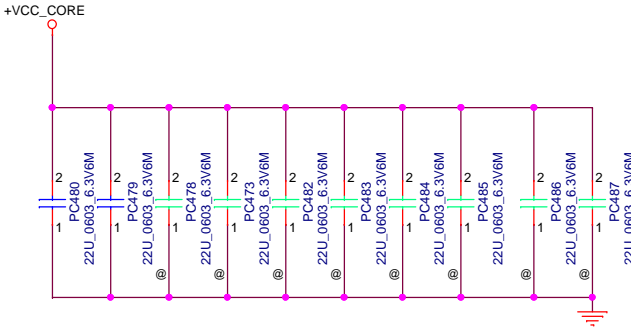
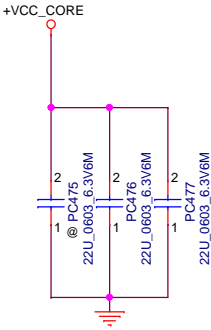
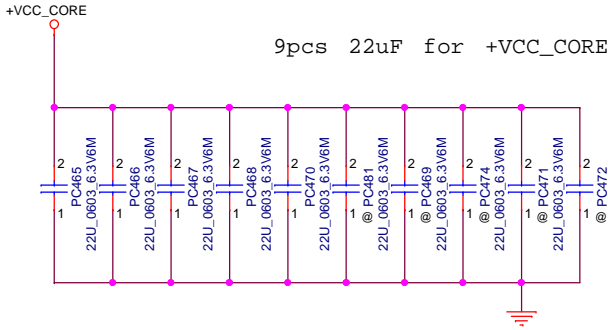
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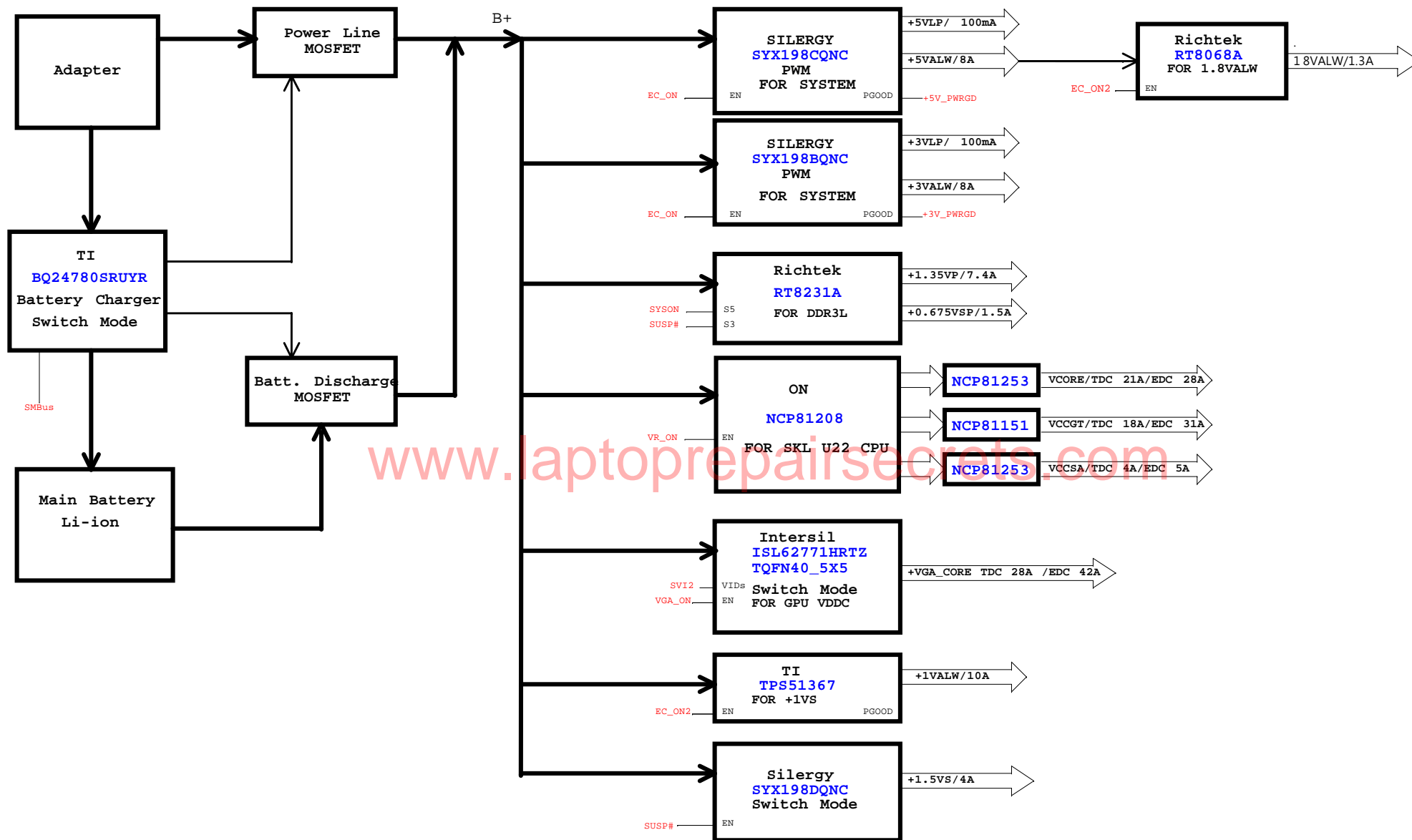


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